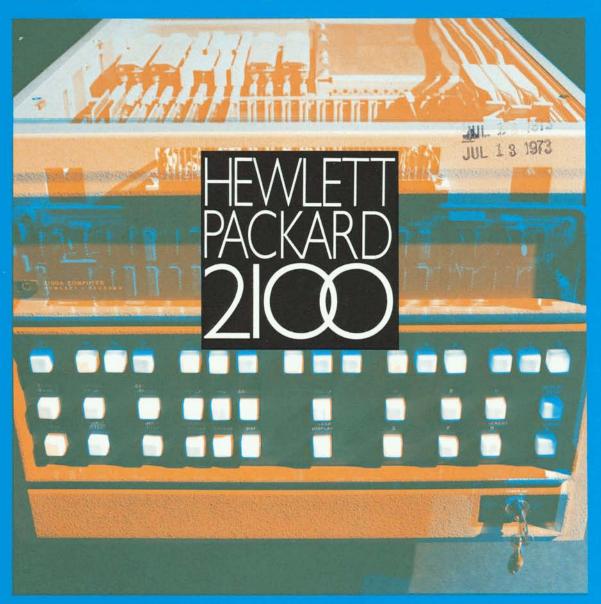
## **Processor description**



HEWLETT hp PACKARD



## The 2100 is designed to fit a variety of needs.

A computer is an effective problem-solver only when it adapts easily and inexpensively to the problems of the outside world. The debate of one specification over another is relevant only to the specific problem. The 2100 was designed so that you can tailor your configuration with proven software and peripherals. And, with writeable control store you can easily enhance the instruction set of the processor to optimize your programs. So when you need it, the 2100 can be customized to solve a particular problem.

All these capabilities are provided without sacrificing the features of a general-purpose minicomputer. Standard equipment includes 80 powerful instructions, hardware multiply/divide, memory protect, power fail with automatic restart, unlimited levels of indirect addressing, 14 I/O channels, and many more. Sub-microsecond 16-bit core memory expandable in the mainframe to 32K of words, parity check and two addressable accumulators. Plus when you want, direct memory access and floating point hardware can be optionally added.

The I/O structure of the computer is designed so a single interface card is all that is usually needed to interface to a peripheral or instrument. Hewlett-Packard offers cards to interface to over 30 HP supported peripherals and over 100 scientific instruments. And, general-purpose interface cards are available so that your special instrument or peripheral will have inexpensive access to the 2100.

Software—we have it. Standard languages include, FORTRAN II and IV, Assembly Language, ALGOL, and HP Extended BASIC. For your application needs, a library of over 500 user-contributed routines are available. HP software has been field tested in over 4000 installations. It provides proven capability with complete documentation.

The 2100 is the processor of a number of HP computer systems. These include time-sharing, a disc operating system, a real-time executive, medical systems, test systems and data acquisition systems. All are fully supported with a dedicated staff of sales engineers, field analysts, and service personnel.

CAUTION
HAZARDOUS VOLTAGE UNDERNEATH
115VAC/230VAC

370 55A

8K

02100 60052

8 8

SSA XVD

8K

ZVD ZGA

8K

02100

SSA

8 K

02100-

CAUTION
HAZARDOUS VOLTAGE UNDERNEA

CONTROL AND STATUS

Power Supply

Memorey

Processor

Space for 14 I/O interface boards

### Check these operating features.

The basic 2100 minicomputer comes equipped with 70 basic instructions plus 10 extended arithmetic instructions. It also includes memory parity check with interrupt, power fail interrupt with automatic restart, and memory protect.

Optional features include incremental memory, direct memory access, multiplexed I/O, floating point instructions, writeable control store, and the ability to write programmable ROM s.

Power Fail Interrupt with Automatic Restart: A standard feature on the 2100 provides insurance against the loss of register data in the event of a power failure.

Priority: Highest priority interrupt.

Power Failure: Detects power failure and generates an interrupt to the trap cell for the user-written power failure routine which saves register contents, terminates activities and halts the processor. A total of 500 microseconds are available for the routine.

Power Restart: Detects resumption of power and generates an interrupt to the trap cell for user-written restart program.

Memory Parity Check with Interrupt: Another standard 2100 feature provides an extra margin of safety for programs and data. Priority: Second highest priority interrupt (shared with memory protect).

Operation: Monitors all words read from memory.

Interrupt: To trap cell for user written routine when parity error is detected.

Violation Register: Contains memory address where error occurred.

Memory Protect: Standard on the 2100. Gives the security necessary to protect a defined area of memory from alteration by a user program.

Priority: Second highest priority interrupt (shared with memory parity).

Operation: Initiated under program control; protects any amount of memory.

Fence Register: Set under program control; memory below fence is protected.

Interrupt: To trap cell for system routine when user program:

- a) Attempts to alter a protected location
- b) Attempts to jump into the protected area
- c) Attempts to execute an I/O instruction Violation Register: Contains memory address of violating instruction.

I/O System: Provides 14 I/O slots in the mainframe. For large system applications an optional extender provides 31 additional slots with supplemental power.

Direct Memory Access: Two DMA ports are built into the 2100. The DMA option provides program assignable word count and address registers which allow standard interfaces to access memory directly through these ports.

Number of Channels: 2

Registers per Channel: Word Count

Register and Address Register

Word Size: 16-bits

Maximum Block Size: 32,768 words Assignment: To any I/O channels

Transfer Rate: Greater than 1 million words

per second

Priority: Channel 1 is higher than Channel 2.

Both are higher than the CPU.

Multiplexed Input/Output: This option provides all signals necessary to implement up to 56 levels of interrupt priority external to the mainframe. Thirteen I/O channels are still available in the mainframe for standard interfaces.

Memory: Ranges from 4K to 32K.

Type: Folded planar core

Word Size: 16-bits with 17th parity bit

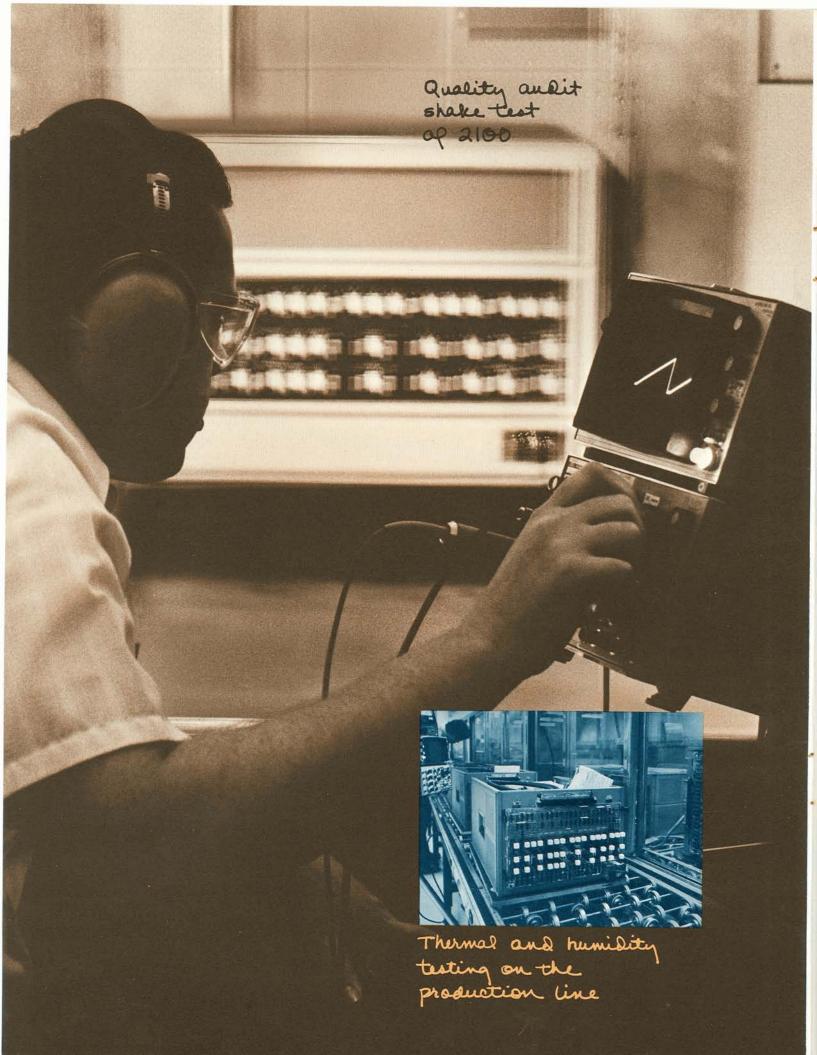
Page Size: 1024 words Direct Addressing: 2 pages Indirect Addressing: All pages

Module Sizes: 4K and 8K word memory modules provide 4K, 8K, 12K, 16K, 24K and 32K configurations all in the 2100A mainframe without additional power supply or cabinetry.

Cycle Time: 980 nanoseconds

Loader Protection: Switch protects last

64 words.



### With every 2100– traditional HP reliability.

The standard HP 2100 is one of the toughest computers ever built. It is designed to go to work where you need it. At oven temperatures in the desert or down to a chilly 32 degrees Fahrenheit, the 2100 can assure you reliable operation. We know this because every 2100 is subjected to a production line thermal cycle. Plus, we maintain a program of periodic in-depth quality audit.

**Environmental Specifications** 

Temperature: The 2100 can withstand

non-operating temperatures from —40 degrees to 165 degrees
Fahrenheit. It can operate from

32 degrees to 131 degrees

Fahrenheit.

Humidity: The 2100 is built to withstand

104 degrees Fahrenheit at 95%

relative humidity.

Altitude: The 2100 may be transported to

altitudes of 25,000 feet in non-operating condition and 15,000 feet for operation.

Shock: The quality audit tests the 2100

for 30 G's of shock for 11

milliseconds over a 1/2 sinewave

shape.

Vibration: The 2100 can withstand

vibration of 1g at 44 Hz.

Electrical

Power Requirements: 115V/230V ±10%

47.5 to 66 Hz

Current Available to I/O:

|        | 2100      | 2155     |
|--------|-----------|----------|
|        | Mainframe | Extender |
| +4.85V | 16.8A     | 45.8A    |
| _2V    | 7A        | 19.5A    |
| +12V   | 3A        | 5A       |
| -12V   | 3A        | 5A       |

Dimensions

Width: 163/4 inches (42,5 cm) with adapters

for mounting in 19 inch (48,3 cm) rack

Height: 12<sup>1</sup>/<sub>4</sub> inches (31,1 cm) (rack mounted)

Depth: 2100-26 inches (66 cm) (23 inches

[58,4 cm] behind rack mounting ears)

2155-23½ inches (59,6 cm) (23

inches [58,4 cm] behind rack mounting

ears)

Weight

Minimum: 91 pounds (41 kg) Maximum: 111 pounds (50 kg)

# A powerful instruction set makes it easy to program.

HP 2100 computers have 80 standard instructions. These instructions are grouped into four types: memory reference, register reference, input/output, and extended arithmetic. In addition, six optional floating point instructions are available.

 Memory Reference (14)
 15
 14
 10
 9
 0

 D/I
 INSTRUCTION
 Z/C
 MEMORY ADDRESS

Memory addressing of the HP computer is based on a 1024-word page structure. All memory reference instructions address either the current page or the zero page. Thus, up to 2048 words are directly addressable. The large page size allows compact programs with a minimum of indirect addressing. Registers or accumulators are directly addressable as memory locations 0 and 1, enabling their contents to be added and compared. You can also load from one accumulator into the other.

Instruction time: 1.96 µsec

| Mnemonic | Description   |
|----------|---|
| AND      | "AND" (M) to A; result in A                                     |
| XOR      | "Exclusive OR" (M) to A; Result in A                            |
| IOR      | "Inclusive OR" (M) to A; Result in A                            |
| JSB      | Jump to subroutine, save P                                      |
| JMP      | Jump, unconditionally   |
| ISZ      | Increment (M); skip if result zero (2.94 µsec instruction time) |
| ADA/B    | Add (M) to A or B; result in A or B                             |
| CPA/B    | Compare (M) with A or B; skip if unequal                        |
| LDA/B    | Load (M) into A or B  |
| STA/B    | Store A or B into M; A/B unchanged                              |

### Register Reference (39)

| 15    | 11  | 10        | 9 0                  |
|-------|-----|-----------|----------------------|
| CLASS | A/B | SR/<br>AS | COMBINED INSTRUCTION |

The extensive set of register reference instructions makes it easy to edit character strings, shift data within and between accumulators, test the accumulators for condition (zero/non-zero, positive/negative, odd/even), and clear, set, increment and form the one's and two's complement of the accumulator contents.

Groups of up to 8 register instructions can be combined to form many useful additional instructions as shown in the combining guide.

Instruction time: 1.96 μsec Shift-Rotate Group

| Mnemonic  | Descript   | tion  |   |
|---|--|---|---|
| Combine<br>instruction<br>(Reference  | No operation Clear E (External External | enificant bit of c left shift one c right shift one c right shift on the control one bit ght one bit, sign clone bit with A collect four bits  in a column vecolumns. | eared or B or B with any                      |
| ALS<br>ARS<br>RAL<br>RAR<br>ALR<br>ERA<br>ELA<br>ALF  | CLE  | SLA   | ALS ARS RAL RAR ALR ERA ELA ALF               |
| BLS<br>BRS<br>RBL<br>RBR<br>BLR<br>ERB<br>ELB<br>BLF  | CLE  | SLA   | BLS<br>BRS<br>RBL<br>RBR<br>BLR<br>ERB<br>ELB |
| Alter-Ski   | p Group  |   |   |
| Mnemonic  | Descript   | ion   |   |
| CLA/B<br>CMA/B<br>CCA/B<br>CLE<br>CME<br>CCE<br>SSEZ<br>SSA/B<br>SLA/B<br>INA/B<br>SZA/B<br>RSS | Clear A or B Complement A Clear-Compler Clear E (Exter Complement E Clear-complem Skip if E is zero Skip if sign of A Skip if least sig Increment A/E Skip if A/B is a Reverse skip se   | ment A/B (see ad)  Enent E (set E)  A/B is zero (ponificant bit of B by one zero  | to $-1$ )                                     |

Combining Guide

Combine one instruction in a column with any instructions in adjacent columns.

(References to A and B registers cannot be mixed.) Example: ALS, CLE, ARS is executed in one instruction.

| CLA<br>CMA<br>CCA | SEZ | CLE<br>CME<br>CCE | SSA | SLA | INA | SZA | RSS |
|-------------------|-----|-------------------|-----|-----|-----|-----|-----|
| CLB<br>CMB<br>CCB | SEZ | CLE<br>SME<br>CCE | SSB | SLB | INB | SZB | RSS |

### Input/Output (17)

| 15    | 11  | 10          | 5 0         |
|-------|-----|-------------|-------------|
| CLASS | A/B | INSTRUCTION | CHANNEL NO. |

These instructions are used to control input/output devices, transfer data to and from peripherals, and control the interrupt system. Data can be input and output directly from the A and B accumulators.

Instruction time: 1.96 µsec

| Mnemoni | c Description                         |
|---------|---------------------------------------|
| HLT     | Halt Program                          |
| STF     | Set flag bit of selected I/O channel  |
| CLF     | Clear flag of selected I/O channel    |
| SFC     | Skip if flag clear                    |
| SFS     | Skip if flag set                      |
| MIA/B   | Merge "OR" I/O channel into A/B       |
| LIA/B   | Load I/O channel into A/B             |
| OTA/B   | Output A/B to I/O channel             |
| STC     | Set control bit of selected channel   |
| CLC     | Clear control bit of selected channel |
| STO     | Set overflow bit                      |
| CLO     | Clear overflow bit                    |
| SOC     | Skip if overflow bit clear            |
| SOS     | Skip if overflow bit set              |

### Extended Arithmetic (10)

Memory Reference

| 15 | 14  | 12  | 11  | 10          | 3    | 0   |
|----|-----|-----|-----|-------------|------|-----|
| CL | ASS | 土   | *   | INSTRUCTION | (ZER | OS) |
| D/ | I   | MEN | 1OR | Y ADDRESS   |      |     |

Register Reference

11 10

| 10    |   | 10 |              |          |       |
|-------|---|----|--------------|----------|-------|
| CLASS | 土 | ** | INSTRUCTIONS | NO. OF S | HIFTS |

Provides hardware implementation of multiply/divide, double load/store, and long shifts and rotates.

Instruction Times:

Extended Arithmetic Instruction

Multiply: 10.7 µsec Divide: 16.7 µsec Double Load: 5.9 µsec Double Store: 5.9 µsec

Shift/Rotate: 2.9 to 7.8  $\mu sec$  dependent

on type and length

| Mnemoni | c Description                           |
|---------|---|
| MPY     | Multiply                                |
| DIV     | Divide                                  |
| DLD     | Double Load                             |
| DST     | Double Store                            |
| ASR     | Arithmetic Shift Right                  |
| ASL     | Arithmetic Shift Left                   |
| RRR     | Rotate B and A Registers Right          |
| RRL     | Rotate B and A Registers Left           |
| LSR     | Logically Shift B and A Registers Right |
| LSL     | Logically Shift B and A Registers Left  |

### Floating Point (optional) (6)

| 15  | 14            | 8        | 1 ( |
|-----|---------------|----------|-----|
| SGN | MANTISSA      |          |     |
| MAN | TISSA (cont.) | EXPONENT | SGN |

The floating point option for the 2100 provides 6 additional arithmetic instructions which are implemented by the microprocessor. This substantially increases the performance of all floating point instructions and subroutines.

#### Instruction times

 Add:
 23.5 μsec to 59.8 μsec

 Subtract:
 24.5 μsec to 60.8 μsec

 Multiply:
 33.3 μsec to 41.1 μsec

 Divide:
 51.9 μsec to 55.9 μsec

 Fix:
 5.9 μsec to 8.8 μsec

 Float:
 9.8 μsec to 24.5 μsec

| Mnemonic | Description |     |     |  |
|----------|-------------|-----|-----|--|
| TAD      | THE ST      | 100 | - 4 |  |

FAD Floating point addition
FSB Floating point subtraction
FMP Floating point multiplication
FDV Floating point division

FIX Fixed point to floating point conversion FLT Floating point to fixed point conversion

\*Word Format Symbols Used

D/I Direct/Indirect: Z/C page zero/current; A/B Register or Accumulator identifier;

SR/AS Shift Rotate/Alter-Skip Identifier

± Instruction Bit

# Class Bit

# A proven architecture is made more flexible with microprogramming.

The 2100's architecture is implemented in a unique manner. It uses the latest in MSI/LSI technology and has retained compatibility with earlier HP computers. This was accomplished by the use of a microprogrammed control section.

The heart of the 2100, the Control Section, directs all the processor operations. It is a computer within a computer having its own registers, 1024 words of 24-bit semiconductor memory, and a cycle time of 196 nanoseconds. The microprogrammed instruction set of the processor resides in the memory of the control section. With this, the user can add instructions easily by adding more read-only-memory or writeable control store.

The ROM address mapper finds the starting address of each microprogram. The microprogram controls the other sections of the processor. These are the arithmetic logic section, I/O section and memory section. The control signals are created by the ROM decoder which interprets each microprogrammed instruction.

The Arithmetic Logic Section performs the instructions commanded by the control section. It includes nine general-purpose registers and the arithmetic logic unit. Four registers (A, B, Q, F) can be gated on the R Bus. And

five registers (P and four scratch pads) can be gated on the S bus. In addition, the R bus can be gated onto the S bus. The S bus provides the main communication path within the 2100. It connects memory and I/O with the arithmetic logic section. Both the R and S bus are input to the function generator which performs the arithmetic and logical function of the computer. The output of the function generator can be stored in any of the nine general-purpose registers using the T bus.

The Memory Section uses a folded planar core memory with a 980 nanosecond cycle time. It is organized into words, pages, and modules. There are 17-bits to a word, 16-bits for instruction or data and one for parity. Page size is a large 1024 words. 4K or 8K modules are available, allowing the 2100 to be expanded from 4K to 32K words.

The Input/Output Section of the computer takes the information from the outside world and makes it available to the computer. There are 14 I/O channels in this section along with special control circuits. Direct memory access, an option to the I/O section, moves data directly between the I/O device and memory. The display and switch register are part of the I/O section.

### **Memory Section**

Memory Addresser

Core Memory

Memory Data Register

.............

### **Control Section**

ROM Address Mapper

ROM Address Register

ROM

Instruction Register

Instruction Decoder

R S FM STO SPC SRA SKA

**Control Signals** 

### **Arithmetic Logic Section**

A Register
B Register
Q Register
F Register

R Bus
Function Generator

SPI Register SP2 Register SP3 Register SP4 Register

P Register

### Input/Output Section

Display Register

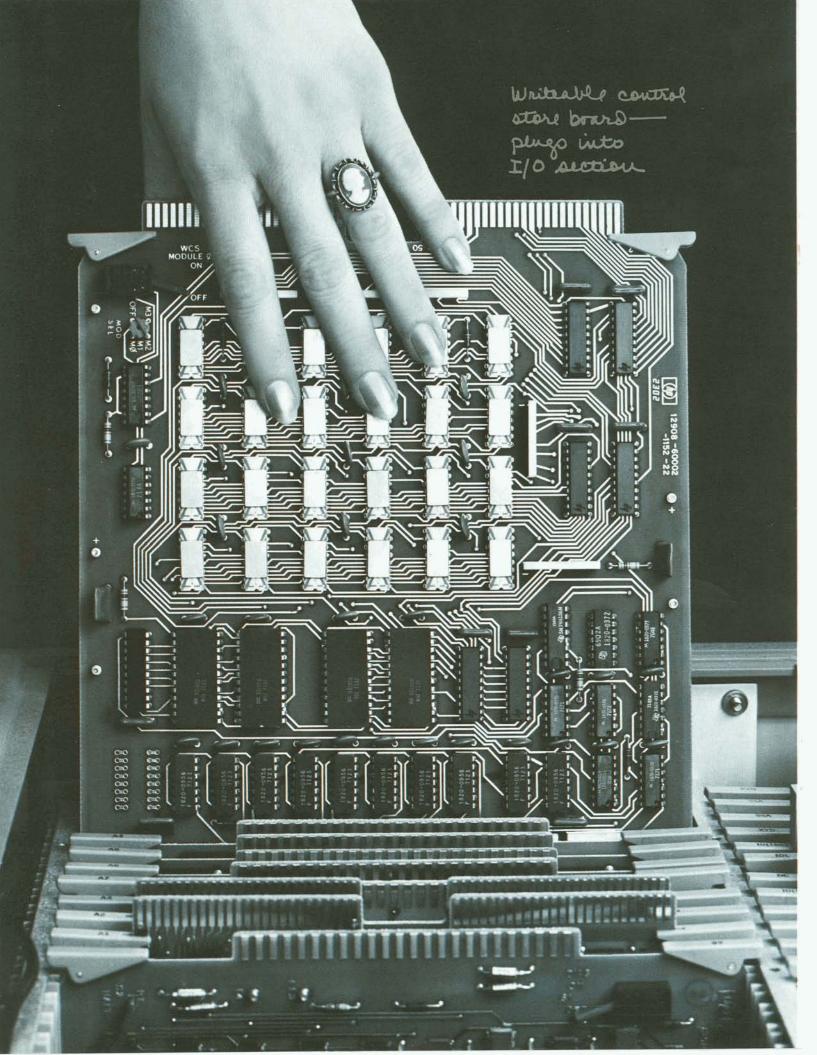
1/O Bus

Interface Cards

T-Bus

Peripheral Device

S Bus



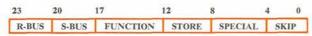
## Microprogramming is easy with writeable control store.

The control section of the 2100 is programmable. The instruction set can be enhanced to meet your specific requirements. The control memory has up to  $1024 \times 24$ -bit words. Only one 256-word section is used by the basic 2100 instruction set. The three other sections are available to you (for custom microprograms or for HP optional instructions). Writeable control store (WCS) is offered to make microprogramming easy. WCS is control memory that can be written on as well as read.

Until now ROM's have been costly and difficult to program, debug, and build. They had to be specially manufactured with a given set of information. Hewlett-Packard offers writeable control store, a section of control memory, which can be accessed and changed by a user program. WCS greatly decreases the cost of debugging and writing microprograms for a special application. Once the correct memory pattern has been determined with writeable control store, an HP programmable ROM writer can be used to fuse in customer instructions. After this, multiple ROM's can be copied if required. The word format for control memory is different from that of main memory.

program in a special symbolic language. The HP micro-assembler accepts punched cards or tape and produces an interim punched tape or disc file and a microprogram listing. This interim tape or file is then processed by a microprogram editor. Depending on the desired end result, the HP loader-editor will give you either a partially or fully loaded writeable control store or a set of mask tapes. The loader-editor is the primary debugging tool for microprogramming. With WCS, the driver used to originally load the card is callable by user programs. This makes it possible to dynamically alter control storage.

Writeable control store and microprogramming are fully supported by HP. The system comes completely documented with a "Microprogramming Guide" and a microprogramming software package to write your own instructions. Microprogramming can greatly increase the performance of your specialized application program. Difficult or lengthy software routines can be performed as a single instruction. In this way the 2100 can be uniquely adapted to a specific purpose.



Writeable control store is easy to use. A microprogramming assembler allows you to



# You can easily interface to the 2100—with a wide choice of peripherals and instruments.

HP provides and supports a wide range of peripherals and instruments. The 2100 has 14 I/O slots to accommodate these. Here are just some of the many peripherals offered.

<u>Teleprinters</u> are offered in a standard and heavy duty model. The heavy duty version is recommended where use exceeds 5 hours per day.

<u>CRT/Keyboard</u> supplies a visual display of information. For data entry, each unit has an alphabetic and a separate numeric keyboard. The data rate is selectable from 10 to 218 char/sec.

Console/Printer can be used as a console, slow speed printer (30 char/sec) and as a keyboard entry device.

Line Printers are offered in three models. Two 132-column printers are available that operate at 200 and 600 lines/min. An 80-column printer is available that operates at 300 to 1000 lines/min.

For Punched Tape HP offers a 500 char/sec reader and two punches, one that punches at 75 char/sec output and another for 120 char/sec. Both mylar and paper tape can be punched on the 75 char/sec unit.

<u>Card Readers</u> are also available. There is an optical mark reader which accepts either punched or marked cards at 200 cards per minute and a 600-card-per-minute reader which reads punched cards only.

Graphic Plotter provides high speed plotting on blank or preprinted paper up to 11 x 17 inches at speeds up to 20 coordinates per second. Absolute coordinates provide accuracy of better than 40 mils.

Magnetic Tape Drives are available in NRZI and phase encoded format. Seven-track NRZI provides selection of bit densities of 200/556/800 cpi. Nine-track units are 800 cpi NRZI or 1600 cpi phase encoded. Tape speeds from 25 to 45 ips are available.

Moving Head Disc Drives come in three types. One version has a removable cartridge, 1.2 million words, access time of 30 milliseconds. Another version with a fixed disc and a removable cartridge has 2.4 million words of storage and an average access time of 42.5 milliseconds. The other moving-head disc drive has 23 million words of storage on a removable 11-high disc pack. Average access time for this one is 32 milliseconds.

General-Purpose Interface boards are available for special devices. They range from a breadboard with only flag and control circuits to complete ready to use interfaces.

Over 100 instruments can access the 2100. HP systems using instrumentation are serving scientists and engineers all over the world.

# The cornerstone for a variety of HP systems, it speaks many languages.

As one of the largest suppliers of minicomputerbased systems, HP has invested hundreds of man-years in the development of systems software and languages. All have been fieldproven in thousands of customer installations.

#### Systems

Basic Control System—BCS handles loading, relocating, linking of user programs, and library subroutines. Simplifies programming and execution of I/O routines.

Disc Operating System—DOS has big system features like extended file management, program chaining, and a job processor that allows the mixing of FORTRAN IV, ALGOL, and assembly language programs. Up to 47 million bytes of random storage can be accessed.

Real-Time Executive—RTE is a true multiprogramming operating system. It can run a foreground real-time program, while concurrently running background batch.

Time-Sharing—The new 2000E and F are low-cost, multi-access systems. They have all the software necessary to service from 16 to 32 simultaneous users with both public and private libraries. HP Extended BASIC is available for easy programming.

Data Acquisition Systems—Hewlett-Packard has been building measurement and instrumentation systems for more than 9 years. Our computer-based systems are working in science and industry solving the complex problems of measurement and control.

FFT Signal Analyzer System—HP's Fast Fourier Transform Processor represents a significant step forward in the analysis of mechanical and structural vibrations, environmental stress, sonar, and other acoustical studies.

Medical Instrumentation Systems—HP offers a complete medical system integration from the instrument to display of information. HP systems are at work in hospitals and laboratories performing complex tasks like computerized cardiac catherization, ECG interpretation, and many other real-time and

data acquisition tasks.

Analytical Systems—The 2100 is the processor for various analytical systems. They range from sophisticated microwave systems to systems that control and analyze a mass spectrometer and gas chromatograph.

### Languages

FORTRAN—The HP Systems use the American Standards Association FORTRAN II and IV. The 2120 FORTRAN also offers a modified version which makes it adaptable to the business environment. FORTRAN can be used on BCS, DOS, and RTE systems.

ASSEMBLY LANGUAGE—These hardware instructions include machine operation codes and symbolic addressing. The output may be absolute or relocatable. The assembly language features page-free programming, fixed and floating point pseudo operations, and the ability to reserve storage with a COM statement.

ALGOL—This language allows problem description in an internationally defined language. It includes all the major elements described in ALGOL 60 revised report, Communications of the ACM January 63, plus a number of features such as an unrestricted nestling of conditional statements and the intermixing of REAL and INTEGER identifiers.

HP Extended BASIC Time-Sharing Interpreter—The HP 2000 Series uses the HP Extended BASIC interpreter. With HP's Extended BASIC you have all the advantages of the Dartmouth Basic plus useful extensions. For instance, you can do complex matrix operations. Data files can be both random and sequential with a maximum of 16 active files per program. And with the CHAIN statement the programmer is not limited by the amount of memory in core. He has available to him the almost unlimited on-line memory of the disc. With the COMMON statement, program and chained subroutines can use the same undisturbed areas of core. For 8K systems core-based BASIC is also available.



And, it's backed by HP world-wide support.

Qualified computer service and support people have to be available world wide to meet today's applications. In industry, education, science and medicine, Hewlett-Packard computers are performing time-critical tasks. To meet these needs, HP has 172 field offices in 65 countries throughout the world. This network includes 60 service facilities in the United States and Canada, backed by 5 regional offices in major metropolitan areas, and 2 service centers in Europe. These facilities all provide a full spectrum of HP support.

Personnel—HP maintains a worldwide staff of highly skilled computer specialists. Each HP technician is factory-trained and continually updates his skills with training on the latest service techniques. Our technicians are backed by HP's factory service engineers. These specialists have direct access to design and production engineers at HP's 19 manufacturing plants and are available to provide you with consultation and problemsolving in unusual or complicated service situations. And they all are committed to providing you with optimum solutions to your service problems.

Equipment—Each HP service facility maintains an extensive inventory of the latest test instruments, including special equipment developed specifically for servicing and repair of HP systems, computers and instruments.

Training facilities—Customer Data Centers provide in-depth training in both software and hardware. A broad range of courses and training materials are available that have been specially developed for HP customers.

Systems analysts—For your software problems, system analysts are on call to answer questions and to provide software support for HP's systems. They are available to give you the support necessary to make your installation a success.



00250 FAIL PASS SWITCH ROM ENABLED SEGMENT PODO DO DO DO DO CHECKSUM ERROR ENABLE CONTINUE ROM INSTRUCTION RESE SELF. 2100 test set - used by field engineering

HEWLETT hp PACKARD