PDP-1

- Proven solid-state logic circuits
- 100,000 additions per second
- Fully parallel processing
- Multiple step deferred addressing
- Expandable random access core memory
- Exceptionally flexible input-output
- Automatic interrupt – 1 to 16 channels
- Connections for high-speed data channels
- Operates on standard 110 volt power
The DEC Programmed Data Processor-1 is a compact, solid-state, general purpose digital computer offering a combination of speed, flexibility and programming power unmatched by any other commercially available computer in its class. It is easy to install, operate and maintain, since it runs on ordinary 110-volt current, features simplified controls, and has built-in marginal checking to facilitate preventive maintenance... Speed: PDP-1 has five-megacycle, solid-state logic circuits based on Digital’s popular line of high reliability circuit modules, a random access magnetic core memory with a cycle time of five microseconds, and 18-bit fully parallel processing. These design features give PDP-1 a computation rate of 100,000 additions per second, including two calls on memory... Flexibility: PDP-1 is engineered to accommodate a wide variety of input-output equipment without internal machine changes. Standard equipment includes an alphanumeric typewriter for on-line input and output operations, a punched tape reader, a punched tape punch, and single-channel automatic interrupt. Optional equipment includes 16-channel sequence break, 16-inch cathode ray tube display, light pen, card punch control, card reader control, tape unit, and tape control units. In the standard machine, multiply and divide are performed by subroutines augmented by the special instructions “Multiply Step” and “Divide Step.” Fully automatic multiply and divide are available as an option... Programming: PDP-1 is a single address, single instruction, stored program machine operating on 18-bit 1’s complement binary numbers. Other equipment of the customer’s own design may be connected to the computer either through the In-Out Register or an external high-speed data channel. Numerous connections for inputs, outputs, data channel interrupts, and similar devices are provided. Programming features include multiple-step indirect addressing, 12 variations of arithmetic and logical shifting, 15 conditional instructions, and capability for Boolean operation... Physical Features: The Central Processor is housed in three equipment frames. All controls and standard input-output equipment are conveniently located in a fourth equipment frame attached directly to the Central Processor. No special wiring, subflooring or air conditioning is required.
Multiply/Divide Type 10 The order "Multiply Y" forms the double length product of the contents of the In-Out Register and the contents of Memory Register Y. The instruction "Divide Y" forms the quotient of the double length dividend stored in the Accumulator and In-Out Register and the divisor contained in Register Y. Divide normally skips the following instruction. If an overflow occurs, the skip does not occur. Multiplication requires 25 microseconds, and divide takes 40 microseconds.

Memory Module Type 12 Each memory module consists of 4096 18-bit words. A maximum of 12 memory modules can be connected to the PDP-1.

Memory Field Control Type 13 This allows expansion of up to four additional registers.

Memory Field Control Type 14 This allows expansion of up to eight additional registers.

High Speed Channel Type 19 This type of channel provides blocks of words between memory locations as magnetic tape.
INPUT-OUTPUT OPTIONS

Sequence Break Type 20 This automatic interrupt feature allows concurrent operation of several in-out devices and the main sequence. The system has 16 automatic interrupt channels arranged in a priority chain. An interrupt or break can be initiated by an in-out device at any time. When a break occurs, the states of the arithmetic and control elements are automatically stored in memory, and program control is transferred to a routine which deals with the device causing the interrupt.

Visual CRT Display Type 30 This is a 16 inch cathode ray tube display mounted on a separate table. The "Display" command will plot one point on the tube at the position indicated by the Accumulator and the In-Out Register. Plotting a point requires approximately 50 microseconds.

Precision CRT Display Type 31 The operation of this 5 inch cathode ray tube display is similar to that of the Type 30. It comes equipped with a mounting bezel to accept a camera or a photomultiplier device.

Light Pen Type 32 This accessory allows information to be "written" on the cathode ray tube. The pen detects displayed information, and the pen output sets a program flip-flop in the machine each time a pulse of light strikes the pen.

Card Punch Control Type 40-523 This control operates a standard card punching machine. It contains an 80 bit buffer which is loaded from the In-Out Register, using the "In-Out Transfer" command, for each card row punched.

Card Reader Control Type 41-523 This control is for use with standard card reading equipment. It allows the read brush outputs to be directed to the In-Out Register.

Tape Transport Type 50 This is a tape unit with control to read and write IBM 727 and 729 I format tape. Two hundred 7 bit characters of information are stored on each inch of tape, and the tape is read or written at the rate of 75 inches per second.

Programmed Tape Control Unit Type 51 This control transfers information between the computer and the tape one character at a time. All transfer operations, including error checking and assembly of characters into computer words, are performed by routines. The Type 51 allows a choice of tape format, including the IBM Type 729 Mod I.

Automatic Tape Control Unit Type 52 This high speed tape control automatically transfers information between the computer memory and the tape in blocks of characters. It allows computation to continue while the transfer is in process. The Type 52 does automatic error detecting while reading and writing. This includes parity and bit-for-bit checks with the main memory. For rapid tape searching, a preselected number of blocks may be skipped. Tape format is IBM.

Programmed Line Printer and Control Type 61 This is an on-line printing station capable of operating at 150 lines per minute (120 columns per line, 64 characters per column).

Automatic Line Printer and Control Type 62 This is an on-line printing station capable of operating at 600 lines per minute (120 columns per line, 64 characters per column).
PDP-1 is an 18-bit parallel machine employing binary arithmetic. Floating point operations and number base conversion are done conveniently by subroutines supplied with the machine.

PDP-1 is a single address machine. The instruction format includes 5 bits for instruction code, 1 bit for indirect addressing and 12 bits for memory address. Operating times of PDP-1 instructions are in multiples of the five-microsecond memory cycle. Shift, rotate, skip, and operate take 5 microseconds. Add, subtract, deposit, and load are two-cycle instructions completed in 10 microseconds. Multiplication by subroutine takes 325 microseconds on the average, and division requires about 440. Optional high speed multiply and divide take up to 25 and 40 microseconds respectively.

A memory reference instruction which is to use an indirect address will have a ONE in Bit 5 of the instruction word. The original address of the instruction is then used to locate a memory register which contains the address to be used in carrying out the instruction. If this register also has a ONE in Bit 5, the indirect addressing procedure is repeated and a third address is located. There is no limit to the number of times this process can be repeated.

DECAL is the PDP Compiler, Assembler and Linking Loader Program. It features true one pass compiling and assembling, takes advantage of the international ALGOL reference language, and allows compiler and assembler-type statements to be freely intermixed to produce a highly efficient object program. At load time, the main program and associated subroutines are automatically cross-referenced and integrated, compactly arranged, and relocated as desired. DECAL is designed to be easily modified and to act as a bootstrap for introducing facilities for handling floating point arithmetic, generalized subscripting and indexing, address arithmetic, recursively defined macro-instructions, arbitrary computational languages, and generalized Boolean algebra.
# PDP INSTRUCTIONS

## BASIC INSTRUCTIONS

All memory reference instructions (except cal and jda) may use an indirect address. The address parts of lot, opr, shi, and skp are used to specify variations of the instruction.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Code</th>
<th>Explanation</th>
<th>Oper. Time (usec.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>add Y</td>
<td>40</td>
<td>Add C(Y) to C(AC)</td>
<td>10</td>
</tr>
<tr>
<td>and Y</td>
<td>02</td>
<td>Logical AND of C(Y) with C(AC)</td>
<td>10</td>
</tr>
<tr>
<td>cal</td>
<td>16</td>
<td>Equals jda 100</td>
<td>10</td>
</tr>
<tr>
<td>dac Y</td>
<td>24</td>
<td>Deposit C(AC) in Y</td>
<td>50</td>
</tr>
<tr>
<td>dip Y</td>
<td>26</td>
<td>Deposit contents of address part of AC in Y</td>
<td>10</td>
</tr>
<tr>
<td>dio Y</td>
<td>32</td>
<td>Deposit C(IO) in Y of AC in Y</td>
<td>10</td>
</tr>
<tr>
<td>dis Y</td>
<td>30</td>
<td>Deposit instruction part Leave in Y &amp; AC</td>
<td>10</td>
</tr>
<tr>
<td>dzm Y</td>
<td>34</td>
<td>Make C(Y) zero</td>
<td>10</td>
</tr>
<tr>
<td>idx Y</td>
<td>44</td>
<td>Index (add one to)C(Y)</td>
<td></td>
</tr>
<tr>
<td>ior Y</td>
<td>56</td>
<td>Inclusive OR of C(Y)</td>
<td>10</td>
</tr>
<tr>
<td>iot</td>
<td>72</td>
<td>See In-Out Transfer Group</td>
<td></td>
</tr>
<tr>
<td>jda Y</td>
<td>17</td>
<td>Equals dac Y plus jsp Y + 1</td>
<td>10</td>
</tr>
<tr>
<td>isp Y</td>
<td>46</td>
<td>Index and skip if result is positive</td>
<td>10</td>
</tr>
<tr>
<td>jfd Y</td>
<td>12</td>
<td>Jump memory field according to C(Y)</td>
<td>10</td>
</tr>
<tr>
<td>jmp Y</td>
<td>60</td>
<td>Take next instruction from Y</td>
<td>50</td>
</tr>
<tr>
<td>jsp Y</td>
<td>62</td>
<td>Jump to Y and save Program counter in AC</td>
<td>50</td>
</tr>
<tr>
<td>lac Y</td>
<td>20</td>
<td>Load AC with C(Y) with C(AC)</td>
<td>10</td>
</tr>
<tr>
<td>law N</td>
<td>70</td>
<td>Load AC with the number N</td>
<td>50</td>
</tr>
<tr>
<td>law — N</td>
<td>71</td>
<td>Load AC with the number —N</td>
<td>50</td>
</tr>
<tr>
<td>lio Y</td>
<td>22</td>
<td>Load IO with C(Y)</td>
<td>10</td>
</tr>
<tr>
<td>mus Y</td>
<td>54</td>
<td>Multiply step</td>
<td>10</td>
</tr>
<tr>
<td>opr</td>
<td>76</td>
<td>See Operate Group</td>
<td>50</td>
</tr>
<tr>
<td>sad Y</td>
<td>50</td>
<td>Skip next instruction if C(AC) differs from C(Y)</td>
<td>10</td>
</tr>
<tr>
<td>sas Y</td>
<td>52</td>
<td>Skip next instruction if C(AC) is same as C(Y)</td>
<td>10</td>
</tr>
<tr>
<td>shift</td>
<td>66</td>
<td>See Shift Group</td>
<td>50</td>
</tr>
<tr>
<td>skp</td>
<td>64</td>
<td>See Skip Group</td>
<td>50</td>
</tr>
<tr>
<td>sub Y</td>
<td>42</td>
<td>Subtract C(Y) from C(AC)</td>
<td>10</td>
</tr>
<tr>
<td>xct Y</td>
<td>10</td>
<td>Perform instruction in Y</td>
<td>50</td>
</tr>
<tr>
<td>xor Y</td>
<td>06</td>
<td>Exclusive OR of C(AC) with C(Y)</td>
<td>10</td>
</tr>
</tbody>
</table>

## OPERATE GROUP

This is a micro program set of instructions. Thus 
\[ cl + cli + clf = 764207 \] (6 microsec.)

- cla 760200 Clear AC
- clf 760001 Clear selected program flag
- cli 764000 Clear IO
- cma 761000 Complement AC
- hlt 764000 Halt
- lst 762200 Load AC from test word switches
- nop 760000 No operation
- stf 760011 Set selected program flag

## IN - OUT TRANSFER GROUP

The number of variations in this group may be greatly increased for optional or special in-out equipment.

- cdf 720X74 Change data field
- cdf 720X74 Change fields
- cks 730033 Check status
- dpy 73007 Display one point on CRT
- esm 720055 Enter Sequence Break Mode
- lsm 720054 Leave Sequence Break Mode
- ppa 730005 Punch punched tape alphanumeric
- ppb 730006 Punch punched tape binary
- rpa 730001 Read punched tape alphanumeric
- rpb 730002 Read punched tape binary
- rrb 720030 Read reader buffer
- rty 720004 Read typewriter input switches
- ryo 730033 Type out

## SHIFT / ROTATE GROUP

Shift is an arithmetic operation. The sign bit is left unchanged and vacated bits are filled with the sign. Rotate is a logical operation and cycles the bits (including sign) in a closed ring. The number of steps is the number of ONE's in bits 9-17 of the instruction (9 max).

- ral 661 Rotate AC left
- rar 671 Rotate AC right
- rcl 663 Rotate combined AC and IO left
- rcr 673 Rotate combined AC and IO right
- ril 662 Rotate IO left
- rir 672 Rotate IO right
- sal 665 Shift AC left
- sar 675 Shift AC right
- scl 667 Shift combined AC and IO left
- scr 677 Shift combined AC and IO right
- sil 666 Shift IO left
- sir 676 Shift IO right

## SKIP GROUP

Skip next instruction if condition is met.

- sma 640400 Skip on minus AC
- spa 640200 Skip on plus AC
- spl 642000 Skip on plus IO
- sza 640100 Skip on ZERO (=O) AC
- szf 640001 Skip on ZERO flag (1 or Flag 0)
- szo 641001 Skip on ZERO overflow (and clear overflow)
- szs 640050 Skip on ZERO sense switch (S = Switch 0)