

The CRAY X-MP Series of Computers

Cray Research, Inc.



Introducing the CRAY X-MP Series of Computer Systems

Now, Cray Research announces an answer to your expanding computational needs — the CRAY X-MP Series of Computer Systems. The CRAY X-MP Series, with its major innovations in architecture and technology, offers overall system throughput up to five times that of a CRAY-1 S/1000 CPU, and a maximum burst rate up to eight times that of the CRAY-1 for specific cases. At the same time, software compatibility has been maintained between the CRAY X-MP and the CRAY-1 to protect user software investment.

The CRAY X-MP is a powerful multiprocessor system. The mainframe features two identical Central Processing Units (CPUs) and a multiport memory. The dual CPUs allow for both multiprocessor jobs and concurrent independent uniprocessor jobs while sharing a two- or four-million word bipolar Central Memory. Four parallel memory access ports per processor provide over eight times the total usable memory bandwidth of the CRAY-1.

The CRAY X-MP Computer System, with its 9.5 nsec clock cycle time, is the fastest general-purpose computer system commercially available today. The X-MP is capable of an overall instruction issue rate of over 200 million instructions per second (MIPS). Computation rates of over 400 million 64-bit floating point operations (MFLOPS) are possible, and combined arithmetic/logical operations can exceed 1000 million operations per second (MOPS).

A high-performance peripheral device has also been developed for use on the CRAY X-MP. The Solid-state Storage Device (SSD), with its exceptionally high transfer rates, can be used as a fast-access disk device for large datasets generated and manipulated repetitively by user programs. It can also be used by the system for temporary storage of system programs. The SSD is available with 64, 128, or 256 million bytes of storage. Complementing the SSD and enabling its high performance is a broadband channel capable of a maximum burst transfer rate of 10 gigabits per second. Performance improvement factors of up to 200 over disk units are achievable.

The I/O Subsystem, which is an integral part of the CRAY X-MP, also contributes to the new system's outstanding performance. The I/O Subsystem offers parallel disk drive capabilities, I/O buffering for disk-resident and Buffer Memory-resident datasets, on-line tape handling, and efficient front-end system communication. Up to 64 million bytes of Buffer Memory can be configured on the I/O Subsystem, enabling faster and more efficient data access and processing by the CPUs.

The CRAY X-MP...a major new computational resource available now. In the future, Cray Research will emphasize development of multiprocessing architecture as an important technique for increasing processing power.

CRAY X-MP hardware features

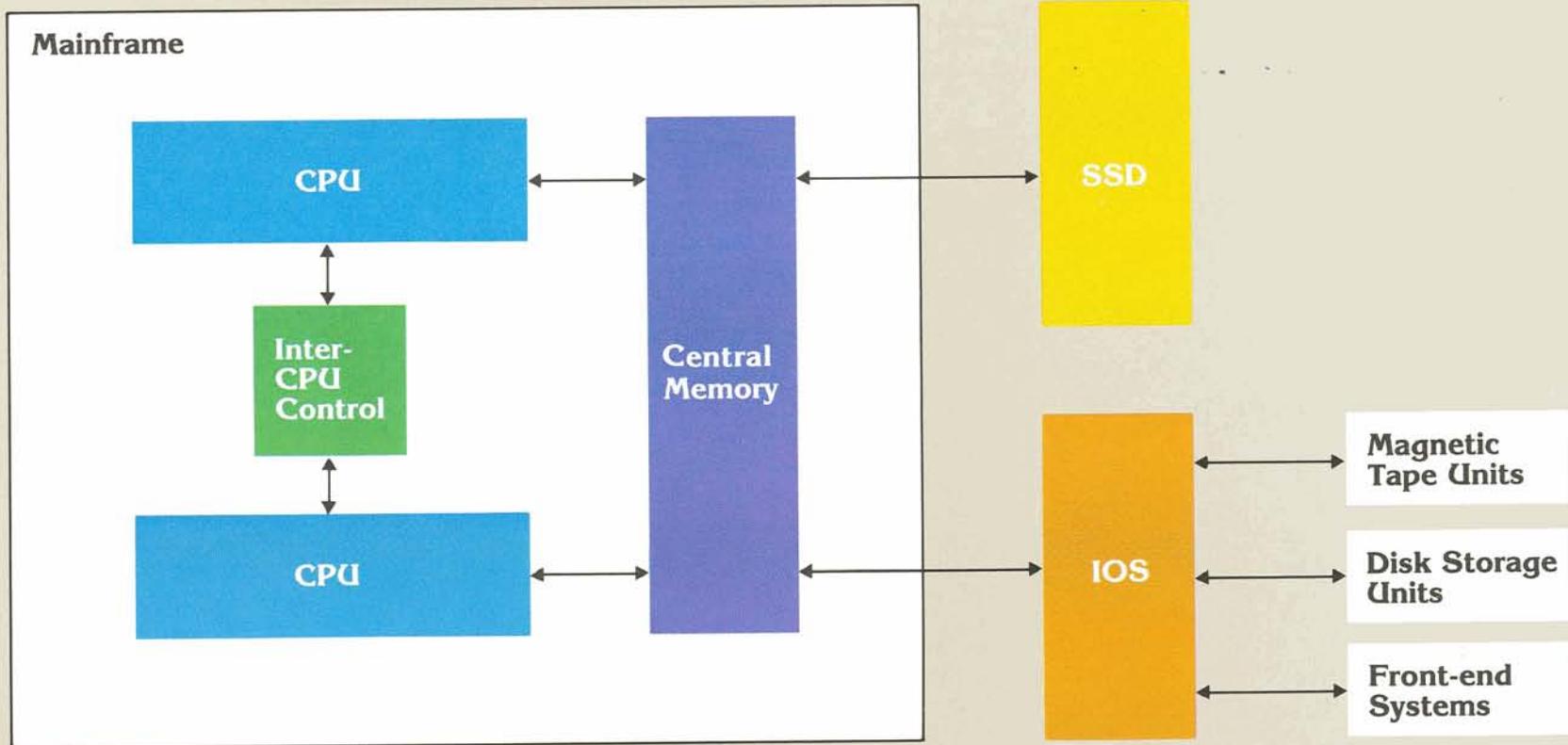
Throughout the CRAY X-MP CPUs, 16-gate array integrated circuits are used. These circuits, which are faster and denser than the circuitry used in the CRAY-1, contribute to a clock cycle time of 9.5 nanoseconds and a memory bank cycle time of 38 nanoseconds. Proven cooling and packaging techniques have also been used on the CRAY X-MP to ensure high system reliability.

The CRAY X-MP's four parallel memory access ports per processor, combined with the improved clock cycle time, means that the CRAY X-MP has more than eight times the total usable memory bandwidth of the CRAY-1.

The high performance of the CRAY X-MP is evident in both scalar and vector modes. Scalar performance is improved through the faster clock, short memory access time, and larger instruction buffers, while vector performance is improved through a combination of faster clock, parallel memory ports and hardware automatic 'chaining' features. These new features allow simultaneous memory fetch, arithmetic, and memory store operations in a series of related vector instructions. Either long or short vector operations, characterized by heavy register usage or heavy memory references, use these features to advantage.

CRAY X-MP software features

The innovative hardware features of the CRAY X-MP are supported by the standard Cray Research software. The CRAY Operating System (COS) supports concurrent independent uniprocessor jobs and multiprocessing of a single job. Multiprocessing can be initiated and controlled from a FORTRAN program, and new techniques extending the multiprocessing capabilities of the CRAY FORTRAN Compiler (CFT) are also being explored.



CRAY X-MP Overall System Organization

The CRAY X-MP Models 22 and 24

The CRAY X-MP Models 22 and 24 are composed of the following basic hardware components.

Two Central Processing Units (CPUs), each with:

- 13 functional units
- A, B, S, T, and V operational registers as in the CRAY-1
- 4 instruction buffers
- 4 concurrent memory ports

Central Memory composed of:

- Either 2M or 4M 64-bit words arranged in 16 or 32 banks, respectively

Input/output channel configuration featuring the following:

- 4 6-Mbyte/sec I/O control channels
- 2 100-Mbyte/sec channels for transferring data between the IOS and Central Memory
- 1 1250-Mbyte/sec channel for transferring data between the SSD and Central Memory

An I/O Subsystem (IOS) identical with that for a CRAY-1 S Series System composed of:

- 2, 3, or 4 high-speed I/O Processors
- 8M, 32M, or 64M bytes of I/O Buffer Memory
- 1 to 8 DCU-4 Disk Control Units
- 2 to 48 DD-29 Disk Storage Units (32 if Block Multiplexer Channel Controller is also configured)
- 1 to 4 BMC-4 Block Multiplexer Channel Controllers
- 1 to 16 Block Multiplexer Channels, which can support user-supplied on-line magnetic tape units
- Operator consoles

An optional Solid-state Storage Device (SSD) with:

- 64M, 128M, or 256M bytes of memory arranged in 16, 32, or 64 banks

A Peripheral Expander providing maintenance functions

Power and cooling equipment

One standard, two optional front-end interfaces

| Model | X-MP/22 | | | X-MP/24 | | |
|---------------------------------------|--------------------|-------|-------|---------|-------|-------|
| Mainframe | | | | | | |
| CPIs | 2 | | | 2 | | |
| Bipolar memory (64-bit words) | 2M | | | 4M | | |
| 6 Mbyte/sec channels | 4 | | | 4 | | |
| 100 Mbyte/sec channels | 2 | | | 2 | | |
| 1250 Mbyte/sec channels | 1 | | | 1 | | |
| I/O Subsystem | | | | | | |
| I/O Processors | 2 | 3 | 4 | 2 | 3 | 4 |
| DCU-4 Disk Control Units | 1-4 | 1-8 | 1-12 | 1-4 | 1-8 | 1-12 |
| DD-29 Disk Storage Units | 2-16 | 2-32* | 2-48* | 2-16 | 2-32* | 2-48* |
| Block Multiplexer Channel Controllers | | 1-4 | 1-4 | | 1-4 | 1-4 |
| Block Multiplexer Channels | | 1-16 | 1-16 | | 1-16 | 1-16 |
| Front-end Interfaces | 1-3 | 1-3 | 1-3 | 1-3 | 1-3 | 1-3 |
| Buffer Memory Size (bytes) | 8M, 32M, or 64M | | | | | |
| Solid-state Storage Device** | | | | | | |
| Memory Size (bytes) | 64M, 128M, or 256M | | | | | |

*16 fewer Disk Storage Units can be configured if Block Multiplexer Channel Controllers are configured.
 **Optionally one per CRAY X-MP.

Highlights

The CRAY X-MP is a powerful computer system ideal for execution of multiprocessor jobs and concurrent independent uniprocessor jobs. With its advanced design and improved performance, the CRAY X-MP offers:

- Overall system throughput up to five times that of a CRAY-1 S/1000 CPU on many jobs, with a maximum burst rate up to eight times that of the CRAY-1 for specific cases
- Two identical Central Processing units sharing a Central Memory of up to four million 64-bit words
- Four parallel memory access ports per processor providing over eight times the total usable memory bandwidth of the CRAY-1
- Four instruction buffers per processor with a combined capacity of 512 16-bit instruction parcels, twice the capacity of those on the CRAY-1
- Operational registers and functional units compatible with the CRAY-1
- Hardware support for partitioning of memory fields into data and program areas
- The new high-performance Solid-state Storage Device (SSD) which, with its transfer rate of up to 10 gigabits/second, can be used as an exceptionally fast-access disk device
- An integral I/O Subsystem that efficiently performs input/output functions between the mainframe, peripheral devices, and the front-end systems and has a sustained transfer rate of up to 90 Mbytes/second between the mainframe and the I/O Subsystem.
- Software that takes advantage of the unique CRAY X-MP hardware features while remaining compatible with that of the CRAY-1
- Compact size—just 100 square feet of floor space required for the mainframe
- Proven component and cooling technologies designed for high reliability

Two Central Processing Units

I/O Subsystem

Central Memory with either 2M or 4M 64-bit words

Field upgradability

One 1250 Mbyte channel for SSD linkage

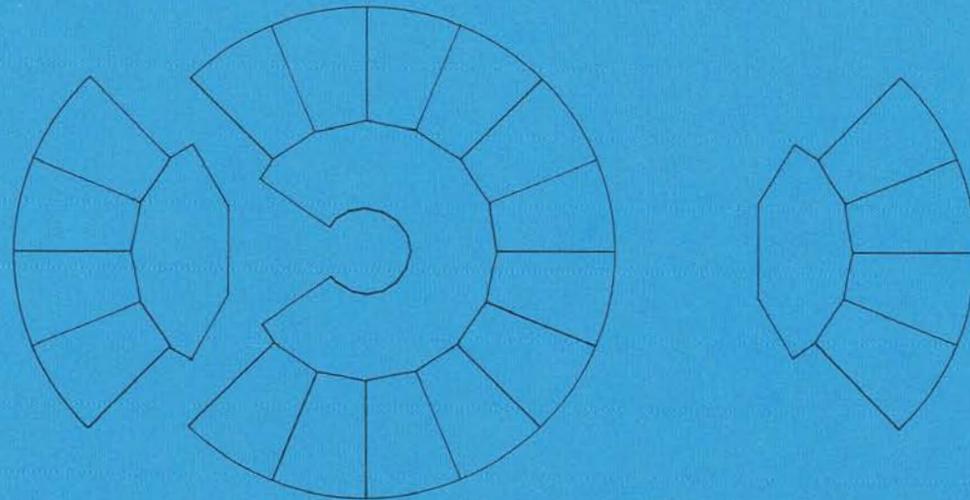
Two 100 Mbyte channels for I/O Subsystem data transfers

Four 6 Mbyte channels for I/O control

Up to 16 Block Multiplexer Channels

Up to 48 DD-29 drives each with a 600 Mbyte capacity

Optional Solid-state Storage Device (SSD)



SSD

Mainframe

IOS

Software for the CRAY X-MP

The processing potential of the CRAY X-MP Series has stimulated the development of new system and user software techniques. Cray Research is committed to providing users with full and easy access to the power of the new CRAY X-MP.

Cray Research software will evolve through planned stages to support multiprocessing capabilities and improved user access to the unique features of the CRAY X-MP, thus achieving greater processing speed of user code. Software products, including the CRAY Operating System (COS), FORTRAN Compiler (CFT), Cray Assembler Language (CAL), and the associated libraries have been enhanced to take advantage of the CRAY X-MP hardware features. All CRAY-1 source code and almost all binary code is upward compatible with the CRAY X-MP. The only exception is binary code that uses the vector functional unit recursion capability available on the CRAY-1.

The CRAY Operating System (COS), by providing the same user interface to both the CRAY X-MP and CRAY-1, enables a smooth migration path to the higher capacity CRAY X-MP systems. COS treats the multiple processors of the CRAY X-MP symmetrically, that is, COS and user code may execute on either processor.

The CFT library allows user partitioning of an application into concurrently executed tasks. Techniques are also being explored for automatic compiler partitioning of a program for multiprocessing.

Special multiprocessor communications and control instructions are also available through the CRAY Assembly Language (CAL) and enable maximum exploitation of the hardware features of the CRAY X-MP.

New software also supports the Solid-state Storage Device (SSD) and I/O Subsystem Buffer Memory so that to users, SSD and Buffer Memory appear like disks. That is, temporary datasets, employed by user jobs, may reside wholly or partially within the SSD or IOS Buffer Memory, resulting in significant reductions of I/O wait time. Use of SSD or Buffer Memory resident datasets does not require changes to user code or to the subroutine libraries; all logical I/O requests are device-independent.

Software Summary

- CFT, a vectorizing and optimizing ANSI '77 FORTRAN compiler
- The FORTRAN subroutine library
- A scientific subroutine library
- A Cray Applications Software Library of public domain software offered as a service
- The Cray Assembly Language (CAL), providing access to all hardware capabilities
- COS, a multiprogramming and multiprocessing operating system
- A variety of system utility programs
- A number of station software service packages that provide full software support for communications between the CRAY and front-end computers
- SSD resident and IOS Buffer Memory resident datasets



The Design of the CRAY X-MP

The CRAY X-MP Mainframe

At the heart of the CRAY X-MP Series mainframe are two identical CPUs, each of which, through various hardware enhancements, is even more powerful than the CRAY-1 uniprocessor. Synchronization of the processors is achieved through clusters of shared registers in the CPU Intercommunication Section and through shared Central Memory.

The CRAY X-MP mainframe is a composite of several key hardware features: a 9.5 nsec clock, two CPUs each with its own computation and control sections, a CPU intercommunication section, a single multiport, bipolar Central Memory, and an I/O section.

The elegant and compact CRAY X-MP mainframe consists of 12 vertical columns arranged in a 270° arc; each column houses two chassis holding up to 72 modules. Power supplies and cooling are clustered around the base and extend outward to provide seating for maintenance personnel.

Physical Characteristics of the CRAY X-MP Mainframe

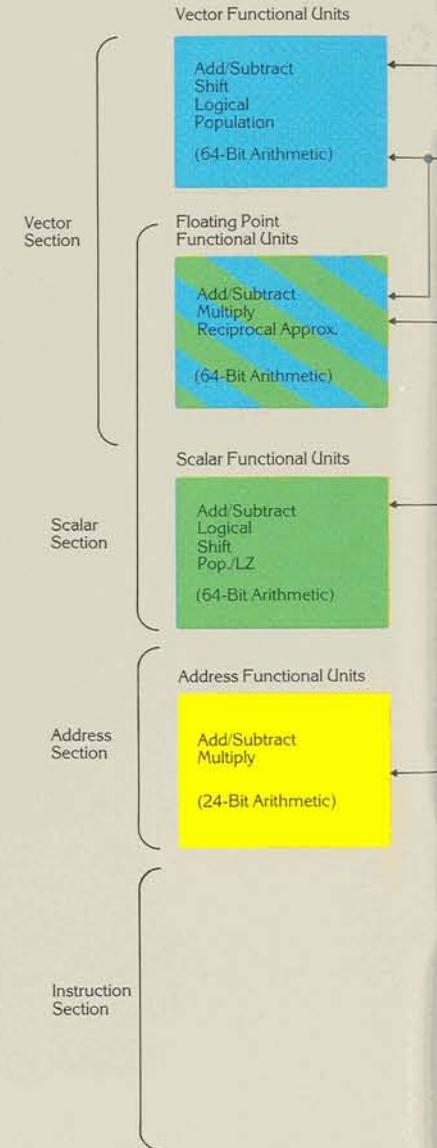
- 100 square feet of floor space for mainframe
- 5.25 tons mainframe weight
- 9.5 nanosecond clock period
- Liquid refrigerant cooling
- 400 Hz power from motor generators

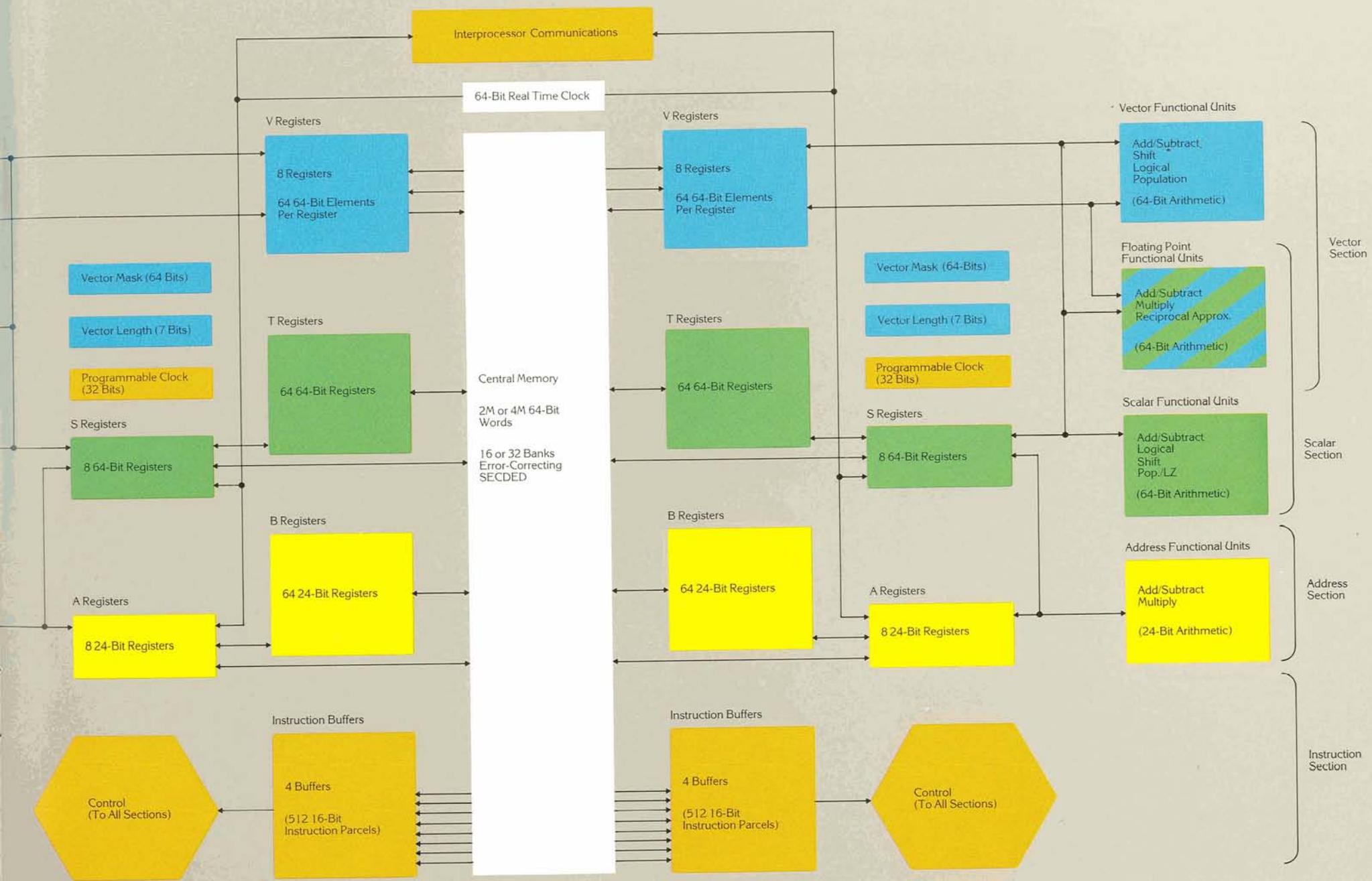
CPU Computation Section

All CRAY X-MP arithmetic operations are bit-compatible with those on the CRAY-1: In fact, the CRAY X-MP's CPUs feature the same set of registers and functional units as the CRAY-1 uniprocessor. However, as explained later, the multiple memory ports available to each CPU in the CRAY X-MP greatly increase the speeds of memory-to-register and register-to-memory transfers over those of the CRAY-1.

CPU Computation Section Summary

- Integer and floating-point arithmetic
- 2's complement integer arithmetic
- Signed magnitude floating-point arithmetic
- Address, scalar, and vector processing modes
- 13 functional units:
 - Vector add/subtract
 - Vector shift
 - Vector logical
 - Vector population count
 - Floating point add/subtract
 - Floating point multiply
 - Floating point reciprocal approximation
 - Scalar add/subtract
 - Scalar shift
 - Scalar logical
 - Scalar population and leading zero
 - Address add/subtract
 - Address multiply
- Eight 24-bit address (A) registers
- Sixty-four 24-bit intermediate address (B) registers
- Eight 64-bit scalar (S) registers
- Sixty-four 64-bit intermediate scalar (T) registers
- Eight 64-element vector (V) registers with 64 bits per element
- 32-bit Programmable clock





CPU Control Section

Each CRAY X-MP CPU contains its own control section. Within each of these are four instruction buffers, each with 128 16-bit instruction parcels, twice the capacity of the CRAY-1 instruction buffers. The instruction buffers of each CPU are loaded from memory at the burst rate of 8 words per clock period.

The contents of the exchange package have been augmented to include cluster number and processor number. Increased protection of data is also made possible through a separate memory field for user programs and data.

Exchange sequences occur at the rate of two words per clock period on the CRAY X-MP.

CPU Control Section Summary

- Four instruction buffers, each holding 128 16-bit instruction parcels
- 128 basic instruction codes
- Exchange sequence mechanism
- Instruction buffers loaded at 8 words per clock period
- Normal and interprocessor interrupt handling
- Separate program and data field protection in memory

CPU Intercommunication Section

The CRAY X-MP CPU intercommunication section comprises three clusters of shared registers for interprocessor communication and synchronization. Each cluster of shared registers consists of eight 24-bit shared address (SB) registers, eight 64-bit shared scalar (ST) registers, and thirty-two 1-bit synchronization (SM) registers. Under operating system control, a cluster may be allocated to both, either, or none of the processors. The cluster may be accessed by any processor to which it is allocated in either user or system mode.

A 64-bit real-time clock is shared by the processors.

CPU Intercommunication Section Summary

- 3 clusters of intercommunications registers, each with:
 - 8 24-bit shared address (SB) registers
 - 8 64-bit shared scalar (ST) registers
 - 32 1-bit synchronization (SM) registers
- A 64-bit real-time clock

Central memory

The CRAY X-MP processors share a single bipolar Central Memory of 2M or 4M 64-bit words that supports the requirements of large-scale applications. Memory is arranged in 32 banks for 4 million word systems and in 16 banks for 2 million word systems. These interleaved memory banks enable extremely high transfer rates through the I/O section and provide low read/write times for vector processing. Finally, the short bank cycle time (38 nanoseconds) is well-suited to high-performance scalar and vector applications.

A major feature of the CRAY X-MP is its four parallel memory access ports per processor, which include two ports for vector reads, one for vector writes, and one for I/O. This notable hardware enhancement provides the CRAY X-MP with over eight times the memory bandwidth of the CRAY-1.

The CRAY X-MP hardware also provides a flexible hardware chaining mechanism for vector processing. This feature enables a result vector to be used at any time as an operand in a succeeding operation. Also, vector chaining to memory as well as from memory is now possible.

Consider the vector triad operation

$$A(I) = B(I) + S * C(I)$$

where S is a scalar, B and C are two input vectors, and A is the output vector. The CRAY X-MP's multiple memory access ports enable two operands to be read and one to be written simultaneously. Thus, the reads of B and C, the multiply, the add and the write into A will all chain together and execute in parallel. In general, the CRAY X-MP enables memory block transfers to the B, T, and V registers in parallel with vector arithmetic operations.

I/O transfers occur at a 2-word-per-clock-period rate, concurrent with CPU memory activities.

Central Memory Summary

- 2M or 4M words of bipolar IC memory arranged in 16 or 32 banks, respectively
- Shared access from the two CRAY X-MP processors
- 4 clock periods (38 nanoseconds) bank cycle time
- 4 memory access ports per CPU
- 64 data bits and 8 error correction bits per word
- Single-bit error correction, double-bit error detection (SECDED)

Memory Transfer Rates

| Source/ Destination | Words per clock period | Total maximum system transfer rate (Mbits/sec) |
|------------------------|---------------------------|--|
| B, T, V | 6 | 40,420 |
| A, S | 1 | 6,730 |
| Instruction buffers | 8 | 53,890 |
| I/O | 2 | 13,470 |

I/O Section

The I/O Section of the CRAY X-MP mainframe, shared by the two CPUs, may be equipped with a variety of high-performance channels for communicating with the mainframe, the I/O Subsystem, and a Solid-state Storage Device (SSD). The CRAY X-MP supports three channel types identified by their maximum transfer rates as 6 Mbytes/sec, 100 Mbytes/sec, and 1250 Mbytes/sec.

Four 6-Mbyte/sec channels are available for communication with the mainframe. In addition, two 100-Mbyte/sec channels are provided. At least one of the 100-Mbyte/sec channels and one of the 6-Mbyte/sec channels must be connected to the I/O Subsystem. The I/O Section is also equipped with a single 1250-Mbyte/sec SSD channel.

To increase CPU efficiency and encourage parallel I/O processing, no peripherals such as disk units are attached directly to the mainframe.

I/O Section Summary

- Four 6-Mbyte/sec channels for communication with the mainframe
 - 16 data bits, 3 control bits, and 4 parity bits
- Two 100-Mbyte/sec channels for data transmissions to/from the I/O Subsystem
 - 64 data bits, 3 control bits, and 8 check bits in each direction
- One 1250-Mbyte/sec channel for use with the SSD
 - 128 data bits and 16 check bits in each direction

I/O Subsystem

The power of the CRAY X-MP is enhanced by the I/O Subsystem (IOS). The IOS with its multiple I/O processors, acts as a data concentrator and data distribution point for the CRAY X-MP mainframe. It can handle I/O for a variety of front-end computer systems and for peripherals such as disk units and user-supplied magnetic tape units.

One of the four I/O processors is always designated as a master processor and is used for communication with all front-end computer systems and for controlling maintenance peripherals. One to three of the I/O processors can each be used for controlling 16 DD-29 Disk Storage Units. Each DD-29 has a capacity of 600 Mbytes. Either one or two of these can be connected to a 100 Mbyte/sec channel between disks and Central Memory. When there are three or more I/O processors in an IOS, one can be designated for block multiplexer control. This IOP supports up to 8 concurrent data streams and up to 64 configurable tape units, 32 of which may be active or assignable at a given time. The tape units supported are IBM-compatible 9-track, 200 IPS, 1600/6250 BPI devices.

The IOS Buffer Memory consists of 8M, 32M, or 64M bytes arranged in 8 or 16 banks, depending on size. It is equipped with single-bit error correction, double-bit error detection (SECDED). Buffer Memories can be upgraded in the field.

The I/O Subsystem is housed in a cabinet that complements the CPU cabinet. Modules comprising Buffer Memory, I/O Processors, and controllers are mounted in four columns arranged in a 90° arc.

I/O Subsystem Summary

- Two to four I/O Processors
- 12.5 nsec clock period
- 8, 32, or 64 Mbytes of Buffer Memory
- Up to 48 600 Mbyte disk storage units
- Optional Block Multiplexer Channels for user supplied tape units
- One to three Cray Research Front-End Interfaces or user-supplied Network Systems HYPERchannel Adapters
- Operator consoles
- A Peripheral Expander and associated maintenance peripherals
- 1.5 tons weight
- 10 square feet of floor space
- Liquid refrigerant cooling
- 400 Hz power from motor generators

Solid-state Storage Device (SSD)

Complementing the CRAY X-MP and designed with its demanding throughput requirements in mind, is the new Cray Research Solid-state Storage Device (SSD). The SSD is available in sizes of 64, 128, or 256 million bytes of on-line storage. Memories are fully field-upgradable from the smallest to the largest sizes offered. Using the latest memory chip technology, the SSD greatly reduces the access and transfer times over that for conventional rotational storage devices.

The SSD connects to the CRAY X-MP mainframe through the specially designed 1250 Mbyte/sec channel so that theoretically the hardware can transfer 8 million bytes of data in 8 milliseconds between the SSD and the mainframe.

The SSD cabinet closely resembles the cabinet of the I/O Subsystem. Similar design to that of the mainframe is used in the power supplies and the liquid refrigerant cooling system. Depending on existing capacities, a site may require additional power and cooling equipment.

Modules are arranged in 16 banks for 64 Mbyte systems, in 32 banks for 128 Mbyte systems and in 64 banks for 256 Mbyte systems. Transfer block sizes are a minimum of 64 words. The memory is fully equipped with single-bit error correction, double-bit error detection (SECDED) logic.

Solid-state Storage Device Summary

- 64 M, 128 M, or 256 M bytes arranged in 16, 32, or 64 banks
- Single-bit error correction, double-bit error detection (SECDED)
- 1250 Mbyte/sec maximum burst transfer rate, assuming 64 banks
- 1.5 tons weight
- 10 square feet of floor space
- Liquid refrigerant cooling
- 400 Hz power from motor generators

Interfaces to Front-end Computers

The CRAY X-MP is interfaced to front-end computer systems through the I/O Subsystem. Up to three front-end interfaces per I/O Subsystem, identical to those used in the CRAY-1, can be accommodated.

Front-end interfaces compensate for differences in channel widths, word size, logic levels, and control protocols, and are available for a variety of front-end systems.

Cray Research Front-End Interfaces

- CDC
- IBM
- Honeywell
- DEC
- Data General
- Systems Engineering Laboratories
- Univac

Users may also elect to supply a Network Systems NSC A130 Channel Adapter in place of one of the front-end interfaces.

Configurations

Flexibility in the choice of an initial configuration and the provision for upgradability to higher capacity systems are hallmarks of Cray Research's complete product family of CRAY X-MP and CRAY-1/S Computer Systems. The CRAY X-MP Series of Multiprocessor Computer Systems broadens the range of possible configurations.

The I/O Subsystem, which is a standard component of CRAY X-MP systems, can be configured in a variety of ways. In particular, the number of I/O Processors may vary from two to four and the amount of Buffer Memory from 8 Mbytes to 64 Mbytes.

Finally, the Solid-state Storage Device is offered for users with the requirement for mass memory of outstanding performance.

Upgradability is a key feature of the CRAY X-MP Series. In addition to upgrading to a maximum of four IOPs in an I/O Subsystem, Central Memory, I/O Subsystem Buffer Memory, and SSD memory are all field upgradable from the smallest to the largest sizes.

An SSD may easily be added to an installed CRAY X-MP system.

CRAY X-MP Maintenance

An extensive set of diagnostic programs is available to field engineers to aid in quickly identifying problem areas in the hardware in event of a failure. These diagnostics are accessed via operator consoles either locally or remotely attached to the I/O Subsystem for technical support.

Further onsite diagnosis to the component level occurs off-line from the mainframe via a sophisticated Cray Research module tester. This is consistent with the CRAY-1 maintenance philosophy of replacing and repairing modules onsite.

CRAY X-MP Reliability

The reliability of the CRAY X-MP, because of the reduced number of components and enhanced cooling system, will meet or exceed that of the CRAY-1, which is recognized as setting a standard in the industry.





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