# The CRAY-1 S Series of Computers

# Cray Research, Inc.



## **Solving Tomorrow's Problems Today**

Weather forecasting and climatology...petroleum research...structural analysis...nuclear research...geophysics and seismic analysis...fluid dynamics...defense...medical research...

Until the advent of the CRAY-1 Computer Systems, solutions to problems in these and many other applications were not possible. The delivery of the first CRAY-1 in 1976 marked a turning point in computing power available. Now, because the CRAY-1 allows greater quantities of data to be processed and derives results more quickly, solutions are not only possible but economically practical as well.

Since its founding in 1972, Cray Research has dedicated itself to the design, development, and marketing of large-scale computers as tools for solving the complex problems facing the scientific, engineering, and technical communities. Science and technology are fields with nearly endless requirements for computing power. Their applications typically call for complex calculations to be performed on large quantities of data. Efficient solution of these sophisticated problems demands very high speed computations and extensive memory. The CRAY-1 Computer Systems are meeting these challenges, solving tomorrow's problems today.

### Some Large-Scale Applications for a CRAY-1

- Weather forecasting and climatology
- Petroleum research
- □ Nuclear research
- □ Fluid dynamics
- □ National defense
- □ Geophysics and seismic analysis
- Structural analysis
- Medical research
- Electrical power distribution
- □ Graphics
- □ Automotive engineering
- Aerospace design
- □ Chemical engineering
- Particle physics
- □ Astronomy
- Economic analysis

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## **The CRAY-1 and Your System**

A CRAY-1 Computer System complements your existing system, serving as a powerful component in a distributed system geared to solving complex problems and handling large amounts of data.

By adding a CRAY-1 to an existing facility you can achieve extremely cost effective computation. Dramatic improvements in throughput are possible when large CPU-bound jobs are off-loaded from your current system onto the CRAY-1. Services such as the operation of slow-speed peripherals may then be handled by a front-end computer operating under control of its own operating system in a mode asynchronous to the CRAY-1.

The CRAY-1 has been successfully interfaced with computers from a number of other manufacturers. A wide variety of computer systems are now serving as front-end processors for CRAY-1 systems.

The CRAY-1 FORTRAN Compiler allows users to take immediate advantage of the CRAY-1's vector processing capabilities, thus preserving the users' investments in FORTRAN programs.

### **Current Front-End Systems for the CRAY-1**

CI		0
C	$\cup$	

□ IBM

Amdahl

Honeywell

DEC
DEC

- Data General
- Systems Engineering Laboratories



(Photo courtesy of Bell Laboratories)

The CRAY-1 Computer System has evolved into the CRAY-1 S Series of Computer Systems. Users have a choice of several models and options. One of the S Series models is sure to meet your specific needs.

At the lower end of the S Series is the Model S/500, which has 512K words of Central Memory. The next larger model differs from the Model S/500 primarily in memory capacity—the S/1000 has 1024K (or 1 million) words. On these two models, front-end computer systems and mass storage link directly to I/O Channels on the CRAY-1 CPU, much as they do on the earlier models of the CRAY-1.

Starting with the S/1200 (also with 1 million words), I/O throughput to front-end computers and to mass storage devices is significantly enhanced with the incorporation of an I/O Subsystem. The I/O Subsystem is a Cray Research product specifically designed to complement the CRAY-1 CPU requirements.

The power of the I/O Subsystem relates directly to the size of Buffer Memory and the number of I/O Processors. Two, three or four I/O Processors may comprise the I/O Subsystem. Two I/O Processors are standard; one or two additional I/O Processors may be added for supporting either additional mass storage or additional Block Multiplexer Channels. Primary features of the I/O Subsystem are Buffer Memory and the incorporation of one or two high-performance channels for streaming data to Central Memory. Cray Research also is developing software to support the attachment of IBM-compatible magnetic tape devices via the I/O Subsystem.

Buffer Memory is a solid-state secondary storage unit accessible to all the I/O Processors in the I/O Subsystem. It may be either 1 million, 4 million or 8 million 64-bit words. Buffer Memory accommodates more and larger I/O buffer areas (up to 1 million bytes each) and allows certain datasets to be memory resident, thus contributing to faster and more efficient data access and processing by the CPU.

Each channel for streaming data to Central Memory enables maximum transfer rates of over 800M bits per second. One bi-directional channel is standard and a second is optional with the I/O Subsystem.

As your computing needs increase, you can expand your system by upgrading your S Series CRAY-1 to a higher model by adding more memory or incorporating a more powerful I/O Subsystem. Upgrading is possible all the way to the Model S/4400, with a maximum of 4 million words of Central Memory, four I/O Processors, and 8 million words of Buffer Memory.

Reliability in hardware and software is a key ingredient in a successful processing environment. The clean architecture of the CRAY-1 is teamed with proven logic circuitry resulting in new levels of hardware reliability. The semicircular mainframe houses over 200,000 integrated circuits, 3400 printed circuit boards, and over 60 miles of wire, yet it takes up less than 70 square feet of floor space. CRAY-1 system up-time recorded in a wide range of production environments is unprecedented for systems of its class.

While you have been reading these lines, somewhere in the world a CRAY-1 Computer System performed several billion calculations. As today's most advanced scientific computer, a CRAY-1 Computer System offers, through its outstanding speed and power, a major computational resource providing new dimensions and capabilities to its users.

Our continuing commitment at Cray Research to be the industry leader of large-scale computer systems is represented by the CRAY-1 S Series, an evolutionary family of field-upgradable systems that can deliver significant price/performance solutions for the scientific and engineering user.

			No. of Lot of Lo	N	and the life of				1000		
odel	S/500	S/1000	S/1200	S/1300	S/1400	S/2200	S/2300	S/2400	S/4200	S/4300	S/4400
CPU Central Memory size (64-bit words)	½M	IM	IM	IM	1M	24	2M	2M	4M	4M	4M
Front-End Interfaces	1-3	1-3	1-3	13	13	1.3	1-3	12		1-3	1.3
I/O Subsystem			dure u- ny 1								avin new contract
I/O Processors			2	1 <b>3</b> 11 mil	4	2		4			4
Buffer Memory Size			1, 4 or 8M	1.4 or 8M	1.4 or 8M	1,4 or 8M	1, 4 or 8M	1.4.or 8M	1.4 or 8M	1.4 or 8M	1, 4 or 8M
DCU-4 Disk Control Units			1-4	1-8	1-12	1-4	1-8	1-12	1-4	1-8	i-12
DD-29 Disk Storage Units			2-16	2.32	2-48	2.16	2-32	2-48	2-16	2-32	2-48
Block Multiplexer Channel Controllers			Prosent.	14	1-4		1:4	1.4		1:4	1-4
Block Multiplexer Channels				1-16	1-16		136	1-16		1-116	1-16
Mass Storage Subsystem											
DCU-3 Disk Control Units	2-8	2-8	Ga-La Santi I								
DD-29 Disk Storage Units	2-32	2-32									

\* 2-32 if Block Multiplexer Channel Controllers are also configured

## CRAY-1 Models S/500 and S/1000

The CRAY-1 Models S/500 and S/1000 systems are composed of a few basic hardware components. These are:

### The Central Processing Unit (CPU) with:

- □ Either 0.5M or 1M words of Central Memory
- □ 12 I/O Channels

## A Maintenance Control Unit composed of:

- A minicomputer
- □ A magnetic tape unit
- □ A removable pack disk drive
- □ A printer/plotter
- □ 2 CRT consoles

## A Mass Storage (Disk) Subsystem consisting of:

- 2 to 8 DCU-3 Disk Control Units
- □ 2 to 32 DD-29 Disk Storage Units

Power and cooling equipment

One standard, two optional front-end interfaces

## **Features**

Front-end interfaces

Memory with <sup>1</sup>/<sub>2</sub>M or 1M 64-Bit Words (4M or 8M bytes)

Field upgradability through the S Series

Disk capacity up to 32 600 Mbyte drives

Disk transfer rates of 4.4 Mbytes/sec.

12 I/O Channels

Software compatibility across the S Series



## CRAY-1 Models S/1200 through S/4400

The CRAY-1 Models S/1200 through S/4400 systems are composed of a few basic hardware components. These are:

### The Central Processing Unit (CPU) with:

- Either 1M or 2M words of Central Memory with 8 banks in 8 columns or 4M words of Central Memory with 16 banks in 12 columns
- □ 12 I/O Channels

### An I/O Subsystem composed of:

- □ 2, 3 or 4 high-speed I/O Processors
- □ 1 or 2 channels for streaming data to Central Memory
- □ 1M, 4M or 8M words of I/O Buffer Memory
- □ 1 to 12 DCU-4 Disk Control Units
- □ 2 to 48 DD-29 Disk Storage Units (2 to 32 if Block Multiplexer Channel Controllers are also configured)
- □ 1 to 4 BMC-4 Block Multiplexer Channel Controllers
- □ 1 to 16 Block Multiplexer Channels
- □ 3 CRT consoles

### A Peripheral Expander connected to:

- □ A printer/plotter
- A magnetic tape unit

Power and cooling equipment

One standard, two optional front-end interfaces

## **Features**

Front-end interfaces

Memory with 1M, 2M or 4M 64-bit words (8M to 32M bytes)

Field upgradability through the S Series

Up to 16 Block Multiplexer Channels

1 or 2 channels with transfer rates of over 800 Mbit/sec each from I/O Subsystem to memory

Disk capacity up to 48 600 Mbyte drives

Disk transfer rates of 4.4 Mbytes/sec.

1M, 4M or 8M words of Buffer Memory

Software compatibility across the S Series

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## **Software for Solving Problems**

Any power is useful only when correctly applied. Accordingly, the design and efficiency of CRAY-1 software supports the hardware computation rates which can exceed 140 million floating-point operations per second.

The CRAY-1's computing power is accessed at two different software levels—FORTRAN and the assembly language—and applied to a broad spectrum of scientific and engineering applications.

All Cray Research software is designed and documented for ease of application, extendability, and maintenance.

Cray Research software has matured with stringent testing at a variety of user sites. It has earned a reputation for both utility and reliability.

### **CRAY-1 Software**

- CFT, a vectorizing and optimizing FORTRAN Compiler
- FORTRAN library subroutines
- CAL, a versatile assembler
- COS, an advanced multiprogramming operating system
- A variety of system utility programs
- Interface software service for IBM MVS and CDC NOS and NOS/BE



CFT makes the tremendous power of the CRAY-1 readily accessible at the user level by removing most of the burden of optimization and vectorization of code.

CFT is a mature compiler. Its development began concurrent with CRAY-1 hardware design in 1973. Now compatible with the ANSI X3.9-1978 FORTRAN Standard, the compiler also accepts most of the older ANSI X3.9-1966 syntax.

The CRAY-1 CFT Compiler automatically generates vectorized machine language code. Thus, the unique features of the CRAY-1 architecture are often exploited at near-optimal rates. The user's investment in FORTRAN program development is therefore protected and the need for costly conversion is eliminated.

A wide range of compiler options has been developed. One feature in particular, Flowtrace, provides the programmer requiring additional optimization with a valuable diagnostic tool. By enabling Flowtrace, the programmer obtains a complete analysis of execution time spent in each subroutine, the number of times each subroutine was called, and subroutine and linkage overhead.

Other compiler options enable listings of assembly code, cross reference maps, and other debugging aids.

Cray Research has made an extensive effort to allow most dialects of FORTRAN and to accept many nonstandard syntax structures that are common in programs written for other manufacturers' equipment.



### **CFT** features include:

- □ Full ANSI X3.9-1978 compatibility
- Acceptance of most dialects and syntaxes implemented for other large-scale computers
- Automatic detection and vectorization of inner loops
- Positive, negative, and zero integer and floating point DOloop indices and limits
- Arbitrary subscript range
- BUFFER IN and BUFFER OUT statements
- □ NAMELIST I/O
- 🔲 Random I/O
- Descriptions of vectorized loops
- Flow analysis, assembly code, cross reference maps, and many other listing and debugging options
- A compilation rate of between 50,000 and 150,000 statements per minute

The CRAY-1 promises to help with exciting breakthroughs in medical and chemical research.

## **Subroutine Library**

The existence of scalar and vector versions of all standard FORTRAN library routines enables CFT to automatically choose the appropriate version.

The possibilities for optimization are further enhanced by SCILIB, a comprehensive library of commonly used mathematical routines. The library currently includes fast Fourier transforms, matrix and linear algebra packages including the widely used LINPACK and EISPACK collections, searches and sorts, and other FORTRAN callable subroutines. Many of these hand-coded routines use the pipeline/chaining properties of the CRAY-1 hardware. These routines are fast—often executing at over 140 million floating-point operations per second—and provide easy access to the full vector power of the CRAY-1.



The CRAY-1 aids in locating and recovering fossil fuels through reservoir modeling and seismic analysis.

## **The CRAY-1 Assembler (CAL)**



The CRAY-1 assembly language enables a user to closely tailor a program to the architecture of the CRAY-1. Through CAL, a programmer may express symbolically all hardware functions of the CRAY-1. CAL allows the production of highly efficient machinelanguage programs. The user may designate program and data information to enable complete control of the CRAY-1 Central Processing Unit.

Augmenting the instruction repertoire is a set of versatile pseudo operations that provide for defining macro instructions and controlling the assembler. CAL applies extensive diagnostics to programs during their assembly and issues error codes where appropriate.

CAL, CFT, the operating system, and most standard software provided by Cray Research are coded in CRAY-1 assembly language.

The CAL assembler, like the CRAY-1 FORTRAN Compiler, is extremely fast. A typical assembly rate is about 250,000 lines per minute.

Complex structural analysis can be visualized in three dimensions using the CRAY-1.

## The CRAY-1 Operating System (COS)

A vital ingredient of the CRAY-1 Computer System is the CRAY-1 Operating System (COS). COS is an advanced operating system offering a multiprogramming batch environment to the user. Up to 63 jobs can be in some stage of processing concurrently.

COS manages all system resources, supervises job processing, and performs input/output operations. The operating system is mostly memory resident (all system utilities reside on mass storage), leaving the bulk of memory available for user jobs. COS is straightforward and uncomplicated.

COS organizes and maintains information on system mass storage. Its dataset management capability provides for the highly efficient creation and maintenance of temporary and permanent datasets, taking full advantage of multichannel access to mass storage.

COS monitors and controls CRAY-1 Computer System resources by allocating memory and mass storage, by scheduling jobs, and by maintaining accounting records.

Jobs and job control information are supplied to the CRAY-1 via a frontend computer or at local or remote job entry stations. Results of CRAY-1 operations, including a logfile of the processed job control statements and accounting information, are returned to the front end or station of job origin.

### Primary features of the Operating System include:

- □ Resource management
- □ Remote or local job entry
- Multiprogramming of up to 63 jobs concurrently
- Recovery of jobs following a system interruption
- Printout of a chronological history (a logfile) of each job
- Communication with station operators
- Staging of data between system mass storage and front-end peripherals
- Program maintenance



## **CRAY-1 Utility Programs**

Utility programs available to the CRAY-1 user include:

- LDR, a relocatable and overlay loader, which allows program modules to be loaded, relocated, and linked to externals in a single pass, and allows redefinition of programs into overlays (separate modules called into execution when necessary)
- □ UPDATE, a program for maintaining program source code
- BUILD, a library generation and maintenance program
- Programs for the management and modification of datasets permanently resident on mass storage
- □ Programs for copying records, files, and datasets
- Programs for positioning datasets relative to records and files
- □ Compare programs
- Dump programs and other aids
- Programs for analyzing the system logfile

The CRAY-1 assists in nuclear process modeling and economic analysis.

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## **The Cray Applications Software Library**

A wide range of available applications software has been implemented on the CRAY-1 Computer System. Both Cray Research, Inc. and CRAY-1 users have participated in this effort. The Cray Applications Software Library service acquires, verifies, documents and distributes to customers public-domain software for the CRAY-1.

Software distributed by the Library is available to all customers of Cray Research, Inc., except where special restrictions have been imposed by the software developer or sponsor.

A complete description of the current Library contents is provided in the "Cray Applications Software Library Catalog." In addition, available documentation accompanies all distributed software.

### The Cray Applications Software Library includes:

- Mathematical and statistical software; for example, equation solution and optimization
- □ Utility software; for example, languages and benchmarking and conversion tools
- Special applications software such as circuit simulation and structural analysis



## **Vendor Software for the CRAY-1**

Currently available vendor software for the CRAY-1 includes:

 Structual engineering MSC/NASTRAN ANSYS STARDYNE

 Nuclear engineering NUCLIB RELAP4/MOD6 PDQ7

- □ Circuit and electronics DRC, ERC META 2.0 HSPICE
- Mathematics and statistics
  IMSL
  NAG
- Fluid dynamics PISCES
- Piping engineering DYNAFLEX
- □ Graphics

DISSPLA CPS-1 PATRAN A substantial and growing number of major applications programs, packages and libraries are available for the CRAY-1 from third party vendors.

In some cases, Cray Research, Inc. has obtained demonstration rights to vendor software. Demonstrations of programs such as MSC/NASTRAN and ANSYS are conducted by Cray Research through the Cray Applications Software Library service.

Vendor software available for the CRAY-1 is identified and described in the "Scientific Applications Package Handbook."

## **Job Flow**

A job may originate from any of a variety of sources local to or remote from your front-end computer. Thus, your existing computers serve as entry stations for submitting jobs to the CRAY-1 Computer System or as data concentrators for multiplexing several remote stations or terminals. Your computer may also provide operator functions by passing commands and messages between the operator and the CRAY-1.

After submission to the CRAY-1, a job waits on mass storage until COS determines that the resources the job needs are available. Then, the system begins job processing by examining the associated job control statements. These statements are read, interpreted, and acted on sequentially. Output from the job is placed on mass storage. At job completion, output is transferred back to the front end or terminal of job origin for additional processing such as printing or transfer to magnetic tape.



<sup>†</sup> The I/O Subsystem and Block Multiplexer Channels are available on Models S/1200 and above.

## **The Design of the CRAY-1**

#### The CRAY-1 Central Processing Unit

From whatever level it is examined, the architecture of the CRAY-1 is clean and simple.

A 6.5 foot high hollow semi-cylinder occupying a mere 70 square feet of floor space, the CRAY-1 challenges the fundamental limitation placed on all computers by the speed of light. By keeping wire lengths short, signal propagation times are minimized. Within the CRAY-1, electronic modules comprising the Central Processing Unit (CPU) lie on the outside of the cylinder; the interconnections are as compact as possible on the inside.

The dense concentration of components requires new techniques to overcome the accompanying problems of heat dissipation. In the CRAY-1, liquid refrigerant is used to maintain internal temperatures of approximately 68° F.

The upholstered benches surrounding the CPU conceal the CRAY-1's power supplies.

Only one physical module type appears throughout the CPU —a module consisting of two 6" x 8" printed circuit boards mounted on opposite sides of a heavy copper heat transfer plate. Each circuit board, in turn, holds a maximum of 144 integrated circuit (IC) packages and approximately 300 resistors. A few basic chip types are used, allowing field inventories for on-site module repair to be small.



Features of the CRAY-1 CPU that contribute to its high speed and reliability include:

- □ Extreme compactness;
- 12.5 nanosecond clock period;
- Vector processing allowing up to 64 pairs of operands to be operated on by a single instruction;
- Random access semiconductor memory that transfers up to 320 million 64-bit words per second while performing single error correction/double error detection (SECDED);
- 13 functional units that operate in parallel to support vector and scalar processing of fixed and floating point arithmetic as well as Boolean and related operations;
- 12 I/O channels which, with associated circuitry, transfer data at speeds determined by the peripheral devices while performing error checking and data assembly/ disassembly; and
- 1 or 2 channels for streaming data (Models S/1200 through S/4400) that allow I/O data transfers directly into memory at rates in excess of 800 megabits per second.

#### **Computation Section**

Within the computation section are operating registers, functional units, and an instruction control network—hardware elements that cooperate in executing sequences of instructions. The instruction control network makes all decisions related to instruction issue

as well as coordinating the three types of processing: vector, scalar, and address. Each of the processing modes has its associated registers and functional units.

The block diagram of the CRAY-1 CPU illustrates the relationship of the registers to the functional units, instruction buffers, I/O channel control registers, and memory.

#### Registers

The basic set of programmable registers are composed of:

- 8 24-bit address (A) registers
- 64 24-bit address-save (B) registers
- 8 64-bit scalar (S) registers
- 64 64-bit scalar-save (T) registers
- 8 64-word (4096-bit) vector (V) registers

Expressed in 8-bit bytes, the CRAY-1 operating registers represent a total of 4,888 bytes of very high speed (6 nanosecond) storage.

The 24-bit A registers are generally used for addressing and counting operations. Associated with them are 64 B registers, also 24 bits wide. Since the transfer between an A and a B register occupies only 1 clock period, the B registers assume the role of cache, storing information for fast access without tying up the A registers for long periods. The 64-bit S registers are used for floatingpoint, logical, and some integer and character operations. The 64-bit T registers act as cache memory for the S registers.

Each of the 8 V registers is actually a set of sixty-four 64-bit registers. The V registers are used for vector operations. Successive elements from a V register enter a functional unit in successive clock periods. The effective length of a vector register for any operation is controlled by a program selectable vector length (VL) register. The vector employed in any calculation need not contain exactly 64 elements. A vector mask (VM) register allows for the logical selection of particular elements of a vector.

In addition to the operating registers, the CPU contains a variety of auxiliary and control registers. These are generally not accessible to a programmer.

#### Addressing

Instructions that reference data do so on a word basis. Branch instructions, on the other hand, reference parcels within words; the lower 2 bits of an address identify the location of an instruction parcel in a word. Significantly, the destination of a jump can be any instruction in the program; word alignment is not required.

#### Instruction Set

The comprehensive CRAY-1 instruction set features over 100 operation codes and provides for both scalar and vector processing. Most instructions occupy 16 bits (1 parcel); certain branch instructions and memory reference operations occupy 32 bits (2 parcels).

Floating-point instructions provide for addition, subtraction, multiplication, and reciprocal approximation. The reciprocal approximation instruction enables the CRAY-1 to have a completely segmented divide operation through performance of a floating-point divide algorithm.

Integer addition, subtraction, and multiplication are provided for by the hardware. An integer multiply operation produces a 24-bit result; an addition or subtraction produces either a 24-bit or a 64-bit result. An integer divide is accomplished through a software algorithm using floating-point hardware.

The instruction set includes Boolean operations for OR, AND, exclusive OR, and for a mask-controlled merge operation. Shift operations allow for the manipulation of 64-bit or 128-bit operands to produce a 64-bit result. Similar 64-bit arithmetic capability is provided for both scalar and vector processing.

A programmer may index throughout memory in either scalar or vector processing mode. This full indexing capability allows matrix operations in vector mode to be performed on rows, on columns, on diagonals and, in general, on any set of data that is stored in memory with regular spacing between elements.

Instructions for population, parity, and leading zero counts (scalar only) return bit counts based on register contents.

#### Instruction Buffers

The CRAY-1 has 4 instruction buffers, each of which holds 64 consecutive 16-bit instruction parcels. The buffers are large enough to hold substantial noncontiguous program segments. Fetching of program steps does not interfere with data or I/O transfer to or from memory.

If a required instruction is not buffer resident, an out-of-buffer condition occurs, causing instructions to be fetched cyclically from the memory banks beginning always with the instruction required for execution. Buffers are loaded from memory starting with the buffer least recently filled at a rate of 4 words per clock period after a 10 clock period startup.

An important feature of the instruction buffers is that both forward and backward branching is possible within them. No reloading of buffers occurs if the instruction being branched to is buffer resident.

#### Data Structure

CRAY-1 internal character representation is in ASCII with each 64-bit word able to accommodate 8 characters.

All integer arithmetic is performed in 24-bit or 64-bit 2's complement mode. Floating-point numbers, 64-bit quantities, consist of a signed magnitude binary coefficient and a biased exponent. The unbiased exponent range is:

 $2^{-20000}$ s to  $2^{+17777}$ s, or approximately  $10^{-2466}$  to  $10^{+2466}$ 

An exponent greater than or equal to  $2^{+20000_8}$  is recognized as an overflow condition and causes an interrupt if floating point interrupts are enabled.

#### Real-time Clock

Programs can be precisely timed with a realtime clock that increments once each 12.5 nanoseconds.

#### Programmable Clock

A programmable real-time clock that has a frequency of 80 Mhz, corresponding to an increment of 12.5 nanoseconds is a standard feature of a CRAY-1 S Series Computer System. This clock allows the operating system to force interrupts to occur at a particular time or frequency.

#### Functional Units

Instructions other than simple transmit or control operations are performed on the CRAY-1 by hardware organizations known as functional units. Each functional unit specializes in implementing algorithms for a specific portion of the instruction set and operates totally independently of the other units. A functional unit performs its operation in a fixed time called the functional unit time. No delays are possible once the operands have been delivered to a functional unit.

All functional units have 1-clock-period segmentation. As a result, information arriving at or moving within the unit is captured and held in a new set of functional unit registers at the end of every clock period. New pairs of operands can then enter the functional unit each clock period even though the unit may require more than 1 clock period to complete the calculation.

All functional units can operate concurrently so that in addition to the benefits of pipelining (each unit can be driven at a result rate of 1 per clock period), there is also parallelism across the units.

The 13 functional units can be thought of as forming four groups: address, scalar, vector, and floating-point. The first three groups act in conjunction with one of the three primary register types to support address, scalar, and vector modes of processing. The fourth group, floating-point, can support either scalar or vector operations and accepts operands from or delivers results to scalar or vector registers accordingly.

#### **CRAY-1 CPU Functional Units**

Unit	Register Usage	Time in Clock Periods
Address functional units		
Addition Multiplication	A A	26
Scalar functional units		
Addition Shift	S	3
Single	S	2
Double	S	3
Logical	S	1
Population, parity and leading zero	S	3
Vector functional units		
Addition	V	3
Shift	V	4
Logical	V	2
Population, parity	V	6
Floating-point functional	units	
Addition	S and V	6
Multiplication	S and V	7
Reciprocal approx.	S and V	14

Interrupts and the Exchange Sequence

Instruction issue is terminated by the hardware upon detection of an interrupt condition. All memory bank and functional unit activity is allowed to complete. To switch execution in order to handle the interrupt, the CRAY-1 executes an exchange sequence. This causes program parameters for the next program to be exchanged with current information in the operating registers.

Each program in the system has associated with it a 16-word block called an exchange package containing the parameters used in its execution sequence. Only the address and scalar registers are maintained in a program's exchange package.

Exchange sequences may be initiated automatically upon occurrence of an interrupt condition or may be initiated voluntarily by the software.

#### **Memory Characteristics**

CRAY-1 Central Memory is large and fast with bipolar LSI chips as its basic elements. It is expandable depending on model type from 512K words to 4 million words. A word is composed of 64 data bits and 8 check bits.

Each memory word is associated with a unique address in memory. The bank cycle time of 50 nanoseconds (4 clock periods) enables 80 million words per second to be accessed in serially addressed blocks. Access time, the time required to fetch an operand from memory to an operation register, is 137.5 nanoseconds (11 clock periods).

Conflict detection and resolution enables simultaneous memory bank operations and prevents the loss of information when bank access conflicts occur. Because of the 4-clock-period memory cycle time, vector memory access can always proceed at one word each 4 clock periods; generally vector memory access is 1 word per clock period.

#### Memory Field Protection

Each object program is assigned a designated field of memory by the operating system. Field limits are defined by a base address register and a limit address register. Any attempt to reference instructions or data outside these limits results in a range error and an interrupt.

Memory field protection assures that no job can inadvertently modify another job in a multiprogramming environment.

#### **CPU** Memory Characteristics

Technology	Bipolar semiconducto				
Word size	72 bits; 64 data 8 SECDED				
Address space	4 million words				
Cycle time	50 nsec				
Size	.5M to 4M words				
Organization	8 or 16 banks interleaved				
Error checking	Single error correction; double error detection				



#### The I/O Subsystem

The CRAY-1 I/O Subsystem has been designed by Cray Research specifically to complement the CPU and to meet its high throughput demands.

By using the I/O Subsystem, mass storage can be expanded to up to 48 disk storage units. Additionally, through use of a Memory Channel, the I/O Subsystem is capable of transferring data directly into memory at extremely high rates without interrupting the CPU.

A Block Multiplexer Channel Controller allows easy addition of other vendors' peripheral equipment. Each controller supports 4 channels.

The Maintenance Peripherals provide for operational and maintenance functions. The I/O Subsystem supports the following components:

2, 3, or 4 I/O Processors

1M, 4M or 8M 64-bit words of Buffer Memory

1 to 12 DCU-4 Disk Control Units

2 to 48 DD-29 Disk Storage Units

3 CRT consoles

1 to 4 Block Multiplexer Channel Controllers

1 to 16 Block Multiplexer Channels

One standard and two optional front-end interfaces

A Peripheral Expander connected to: A printer/plotter A magnetic tape unit



#### I/O Subsystem Functions

Up to 4 I/O Processors comprise an I/O Subsystem. The Master I/O Processor (MIOP) and the Buffer I/O Processor (BIOP) are required: the other 2 processors are designed for moving data at high speeds and are optional. The MIOP connects to the Peripheral Expander, to the CRT consoles, to the CPU (through a normal channel), and to front-end computer systems. The BIOP is connected to 1 or 2 channels for streaming data and moves data between Buffer Memory and Central Memory at rates of over 800 megabits per second. The 2 optional I/O Processors can be 2 Disk I/O Processors (DIOP) for driving additional disk storage units or a DIOP and a Block Multiplexer I/O Processor (XIOP) for controlling other devices. The BIOP and each DIOP contains 1 to 4 DCU-4 Disk Control Units. each of which controls up to 4 DD-29 Disk Storage Units. Similarly, an XIOP contains 1 to 4 Block Multiplexer Channel Controllers, each of which contains up to 4 Block Multiplexer Channels.

The I/O Processors are all connected to each other and to Buffer Memory.

Software for the I/O Subsystem interfaces with the operating system on the CPU. User interfaces are fully compatible for all models in the S Series.

The operating subsystem (Kernel) resident in each I/O Processor:

Handles interrupts,

Controls the disk units and other peripherals such as magnetic tape units,

Supports station and front end activities,

Dispatches messages to and from the CPU,

Handles interprocessor communications, and

Loads overlays.

The Kernel is the same for all I/O Processors and is modified by system parameters at time of installation.

#### **I/O Processor**

Each of the I/O Processors (2 minimum; 4 maximum) is a powerful minicomputer designed specifically for controlling and directing the flow of data at high rates from the CP(I to peripheral devices and other computer systems. The 16-bit computation section is coupled with a fast bipolar local memory. The I/O Processors are ideally suited for mass storage access, network control, and computer interfacing.

Computation section — The computation section consists of registers and functional units having interconnecting data paths. Arithmetic is performed in a single adder in 2's complement mode. Floating-point arithmetic is not incorporated. The 128-instruction repertoire is purposely simple and includes a variety of branching and I/O functions. Shifts are either left or right and circular or end off. Several logical operations are available. Instructions occupy either 16 bits (1 parcel) or 32 bits (2 parcels).

#### **Computation Section Characteristics**

- □ 16-bit parcels
- □ Single address mode
- □ Addition/subtraction unit
- Shift unit
- 9-bit index register
- 512 operand registers
- 32-level instruction stack
- Subroutine return stack
- □ 128 operation codes

*I/O section* — Communication with an I/O Processor is through accumulator channels and through the 6 direct memory access (DMA) ports. Each port is full duplex and transfers a 16-bit data word each clock period. Ports are organized into three groups with a priority scheme within each group. One input port and one output port may be active at the same time as long as the ports belong to different groups. Thus, a DMA port can handle data at a theoretical rate of over 800 megabits per second.

The ports are assigned to I/O Channels, possibly with several channels sharing one port. An I/O Processor includes an addressing capability for up to 512 separate channels; however, hardware restrictions impose a practical limit of 40. The slower the required data rate on the channels, the more channels that may be multiplexed onto one DMA port.

All I/O controlled by the I/O Subsystem originates with the CPU. Status is returned to the CPU to indicate request completion.

#### **I/O Section Characteristics**

- □ 6 full duplex DMA ports
- Over 800 megabits per second per DMA port
- □ 16 data bits
- Program selection of channel number
- Simultaneous input and output
- Interrupt driven under program control

Local memory — The local memory is composed of 65,536 16-bit parcels arranged in 4 sections of 4 banks each of bipolar LSI memory. There are 2 parity bits per parcel. All 16 memory sections are independent. Memory cycle time is 4 clock periods. The access time, that is, the time required to bring an operand from memory, is 7 clock periods.

A significant portion of an I/O Processor's local memory serves as I/O buffers.

#### Local Memory Characteristics

- □ 65,536 16-bit parcels
- 16 banks of 4,096 parcels each
- 4 clock period bank cycle time
- 7 clock period read time
- 1 instruction fetch per clock period
- Odd parity protection (2 parity bits per 16 bits)
- 3 data paths for reading; 2 data paths for writing

#### I/O Subsystem Buffer Memory

Buffer Memory is a separate independent storage unit accessible to all of the I/O Processors in the I/O Subsystem. It is a solid state device composed of NMOS (Negative Channel Metal Oxide Semiconductor) integrated circuits having a capacity of 1.0M to 8.0M 64-bit words.

The I/O Processors connect to the Buffer Memory through 850 megabit ports. For a 1M or 4M word memory, a maximum bandwidth of 1024 megabits per second is possible; for an 8M word MOS memory, a maximum bandwidth of 2048 megabits is possible.

#### **Buffer Memory Characteristics**

#### Data Storage

#### □ 64-bit words

- □ 1.048.576 or 4.194.304 or 8.388,608 words
- 8 banks (1,048,576 or 4,194,304 words) or 16 banks (8,388,608 words)
- 2 millisecond refresh rate
- 200 nanosecond access time
- 375 nanosecond cycle time

#### **Error** Correction

- □ SECDED within memory
- Error data available to separate error reporting channel

#### Interface

- □ 16-bit parcels
- Approximate transfer rate:
  - 1000 Mbits/sec for 1M or 4M memory 2000 Mbits/sec for 8M memory
- Block sizes up to 16K 64-bit words

#### I/O Subsystem Mass Storage

The Buffer I/O Processor (BIOP) and at most two additional Disk I/O Processors (DIOP) can be dedicated to mass storage data transfers. The BIOP differs from a DIOP because it connects to the CRAY-1 CPU via a Memory Channel. Each BIOP or DIOP can have up to 4 DCU-4 Disk Control Units.

#### Each DCU-4 Controller supports up to 4 DD-29 Disk Storage Units. All units connected to a DCU-4 may be active simultaneously and can be directly accessible to the CPU rather than going through CPU memory. However, the number of concurrent data streams is limited by the Buffer Memory size, the BIOP transfer capacity, and software overhead. For example, on a Model S/x200, this limit might be 6 streams while on a larger system, it could be as many as 12 streams.

The DCU-4 Controller used on the I/O Subsystem is a combination of hardware and controlware.

The DCU-4 linkage to the I/O Subsystem is standard for Models 1200 and above.

#### DD-29 Disk Storage Unit Characteristics

Byte capacity	606x10 <sup>6</sup>
Tracks per surface	823
Sectors per track	18
Bytes per sector	4096
Data transfer rate (bytes per second)	4.4x10 <sup>6</sup>
Disk cylinder capacity	0.74x10 <sup>6</sup>
Access time Maximum Adjacent	80 ms 15 ms
Latency	16.6 ms
Recording surfaces	40 per drive
Number of head groups	10

#### Mass Storage Subsystem

A Mass Storage Subsystem is composed of DCU-3 Disk Controllers and DD-29 Disk Storage Units.

The DCU-3 Disk Controllers connect to the CRAY-1 CPU through I/O Channels. Each controller requires 1 I/O Channel and may control up to 4 disk storage units. The DCU-3 Controller is a Cray Research product implemented in ECL logic similar to that used in the CPU. The controller is double-buffered to allow streaming of data to a DD-29 Disk Storage Unit at full hardware rates.

A Mass Storage Subsystem composed of 2 to 8 DCU-3 Disk Controllers and 2 to 32 DD-29 Disk Storage Units is standard on the Models S/500 and S/1000. However, the actual maximum number of controllers and disk storage units depends on the number of available channels; for example, if 4 channels are used for front-end computer systems (including one channel for the MCU), the remaining 8 can be used for a Mass Storage Subsystem that could support up to 32 DD-29 Disk Storage Units.

#### **Magnetic Tape Support**

Cray Research is developing software to support the attachment of IBM-compatible magnetic tape devices directly to certain S Series systems. The magnetic tape devices will attach via the channels of the Block Multiplexer I/O Processor (XIOP). A single XIOP will support up to 8 concurrent data streams and up to 64 total configurable tape devices, 32 of which may be active or assignable at a given time. The tape units supported are IBM-compatible 9-track, 200 IPS, 1600/6250 BPI devices.

### Direct Front-End Link





#### I/O Subsystem Front-End Link

CRAY-1 Models S/1200 through S/4400



#### **Front-end Interfaces**

Each front-end computer system connected to the CRAY-1 executes under control of its own operating system in a mode asynchronous to the CRAY-1. The CRAY-1 is interfaced to frontend systems through special adapters that compensate for differences in channel widths, machine word size, electrical logic levels, and control protocols. These interfaces are Cray Research products implemented in logic compatible with the host system.

Cray Research provides external interfaces to a variety of other manufacturers' equipment. Cray Research is willing to work with customers to develop hardware interfaces for other computers.

The adjoining figures illustrate how front-end computer systems link directly to the CRAY-1 System I/O Channels or through the I/O Subsystem. The normal I/O Channel linkage is standard for Models S/500 and S/1000. The I/O Subsystem linkage is the standard mode for all other models.

#### **Operator Functions**

Operator control of the CRAY-1 is through any front-end computer system designated as the master operator station. The master station operator has available a versatile set of commands for controlling the flow of jobs and data files. A portion of the I/O Subsystem (that is, the CRTs and the maintenance peripherals) can also be designated as the master operator station. The Maintenance Control Unit (MCU) provides similar capabilities for Models S/500 and S/1000. System startup is initiated at the I/O Subsystem (where present) or at the MCU (where present).

#### **Maintenance Functions**

An extensive set of diagnostic programs is available to field engineers to aid in quickly identifying problem areas in the hardware in event of a failure. Where the I/O Subsystem is present, these diagnostics are accessed via the operator consoles and the maintenance peripherals attached to the I/O Subsystem. Where the MCU is an integral part of the system, it serves maintenance functions.

## **Cray Research, Inc.**

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